ST. ANNE'S COLLEGE OF ENGINEERING AND TECHNOLOGY

ANGUCHETTYPALAYAM, PANRUTI-607 110.

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

BE3271 BASIC ELECTRICAL AND ELECTRONICS ENGINEERING LABORATORY MANUAL

I YEAR / II SEMESTER
MECHANICAL ENGINEERING

Prepared by
Mrs. J. Arul Martinal
Assistant Professor
Department of EEE

DOs and DON'T DOs in Laboratory

1. Understand the equipment to be tested and apparatus to be used.
2. Do not touch the live terminals.
3. Select proper type (AC or DC) and range of meters, Use suitable wires (type and size).
4. All the connection should be tight. Do not leave loose wires (i.e. wires not connected).
5. Get the connection checked before switching 'ON' the supply.
6. Never exceed the permissible values of current, voltage, and / or speed of any machine.
7. Switch ON or OFF the load gradually and not suddenly.
8. Strictly observe the instructions given by the Staff / Lab Instructor

LIST OF EXPERIMENTS

1. Verification of ohms and Kirchhoff's Laws.
2. Load test on DC Shunt Motor.
3. Load test on Self Excited DC Generator
4. Load test on Single phase Transformer
5. Load Test on Induction Motor
6. Characteristics of PN and Zener Diodes
7. Characteristics of BJT, SCR and MOSFET
8. Half wave and Full Wave rectifiers
9. Study of Logic Gates
10. Implementation of Binary Adder and Subtractor
11. Study of DSO

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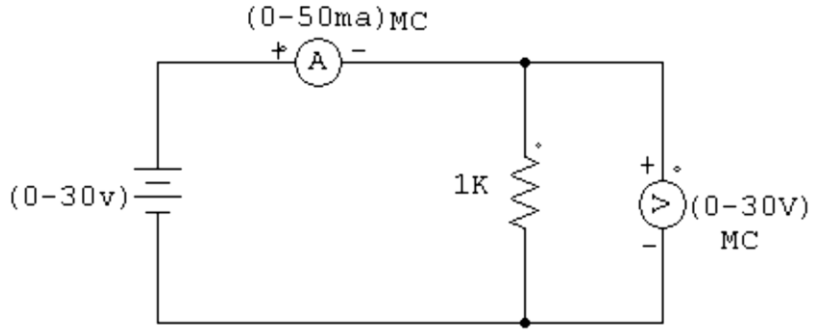
S.NO	DATE	NAME OF EXPERIMENT	PAGE NO	SIGNATURE

Circuit Diagram:



OHM'S Law

S.No.	Voltage (V)	Current (I)	Calculated Resistance (ohm)	Actual Resistance (ohm)

FORMULAE USED:

V=I*R

WHERE V - VOLTAGE

I - CURRENT

R -RESISTANCE

THEORETICAL CALCULATION:

Ex.No.

VERIFICATION OF OHM'S LAW, KVL AND KCL

(a) VERIFICATION OF OHM'S LAW

AIM

To practically verify the ohm's law, for the given electrical circuit with the theoretical calculations.

APPARATUS REQUIRED

Sl.No	Name of the apparatus	Range	Type	Quantity
1	Regulated power supply	(0 - 30) V	Analog	1
2	Voltmeter	(0 - 30) V	MC	4
3	Resistor		1W	3
4	Bread board			1
5	Connecting wires			As Required

Statement:

Ohm's law: Ohm's law states that "At constant temperature, the steady current flowing through the conductor is directly proportional to the potential difference across the two ends of the conductor"**.**

Procedure: -

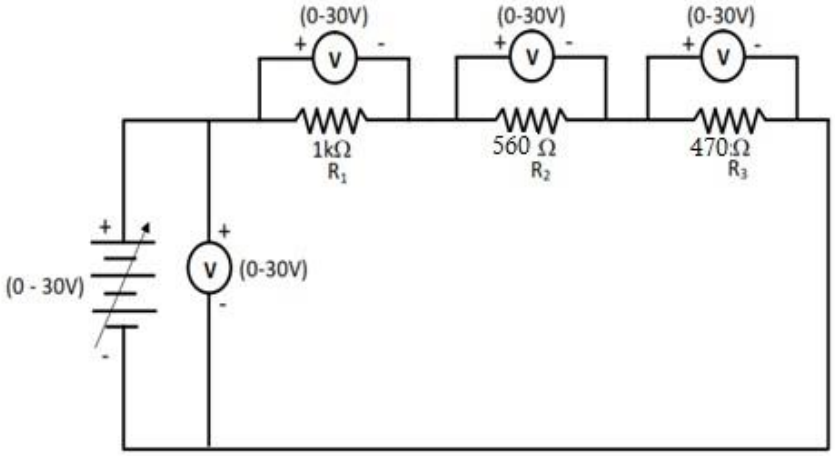
1. Connections are made as per the circuit diagram

2. By Varying the Input Voltage, the voltage and the corresponding current values are noted down for the given Resistor.

RESULT:

Thus Ohm's law has been verified both theoretically and practically.

CIRCUIT DIAGRAM:



TABULAR COLUMN:-

S.No	Voltage (V)	Voltage V1 (V)	Voltage V2 (V)	Voltage V3 (V)	Total voltage Vt = V1+V2+V3 (V)	
					Theoretical	Practical

THEORETICAL CALCULATION:

(b) VERIFICATION OF KIRCHOFF'S VOLTAGE LAW

AIM

To practically verify the kirchoff's voltage law for the given electrical circuit with the theoretical calculations.

APPARATUS REQUIRED

Sl.No	Name of the apparatus	Range	Type	Quantity
1	Regulated power supply	(0 - 30) V	Analog	1
2	Voltmeter	(0 - 30) V	MC	4
3	Resistor			
4	Bread board			1
5	Connecting wires			As Required

KIRCHOFF'S VOLTAGE LAW

In any closed circuit the sum of potential drop is equal to the sum potential rise.

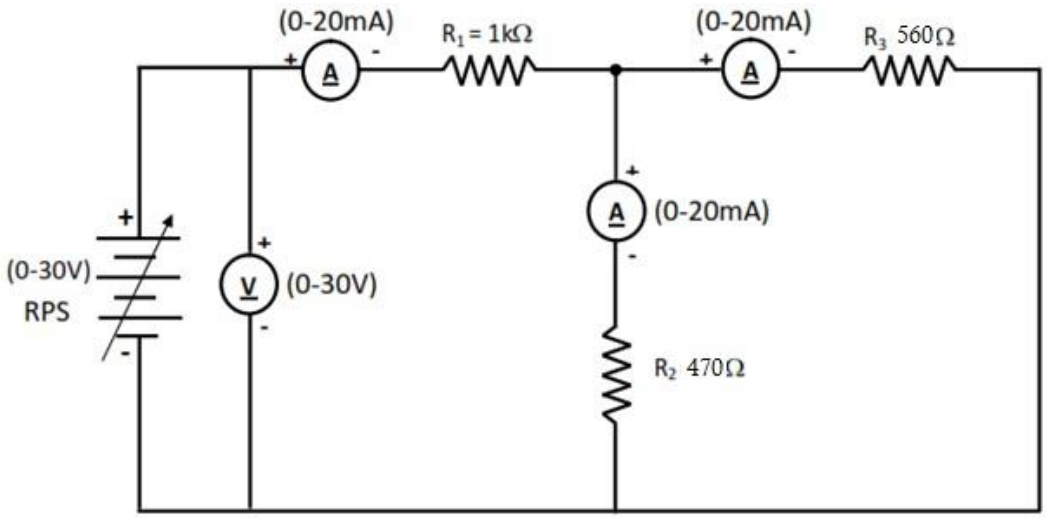
PROCEDURE

1. Make the connections as per the circuit diagram
2. Switch on the power supply
3. Vary the RPS to a specified voltage and note down the corresponding voltage readings across resistors
4. Repeat the above step for various RPS voltages and tabulate the readings

RESULT:

Thus Kirchoff's voltage law has been verified both theoretically and practically.

CIRCUIT DIAGRAM:



TABULAR COLUMN:-

S.No	Voltage (V)	Current I1 (mA)	Current I2 (mA)	Current I3 (mA)	Current I1= I2 + I3	
					Theoretical	practical

THEORETICAL CALCULATION:

(c) VERIFICATION OF KIRCHOFF'S CURRENT LAW

AIM:

To practically verify Kirchoff's current law, for the given circuit with the theoretical calculations.

APPARATUS REQUIRED:

Sl.No	Name of the apparatus	Range	Type	Quantity
1	Regulated power supply	(0 - 30) V	Analog	1
2	Voltmeter	(0 - 30) V	MC	4
3	Ammeter			
4	Resistor			
5	Bread board			1
6	Connecting wires			As Required

KIRCHOFF'S CURRENT LAW

The algebraic sum of the current meeting at any junction or node is zero. In other words, the sum of the current flowing towards a junction is equal to the sum of the current leaving from the junction.

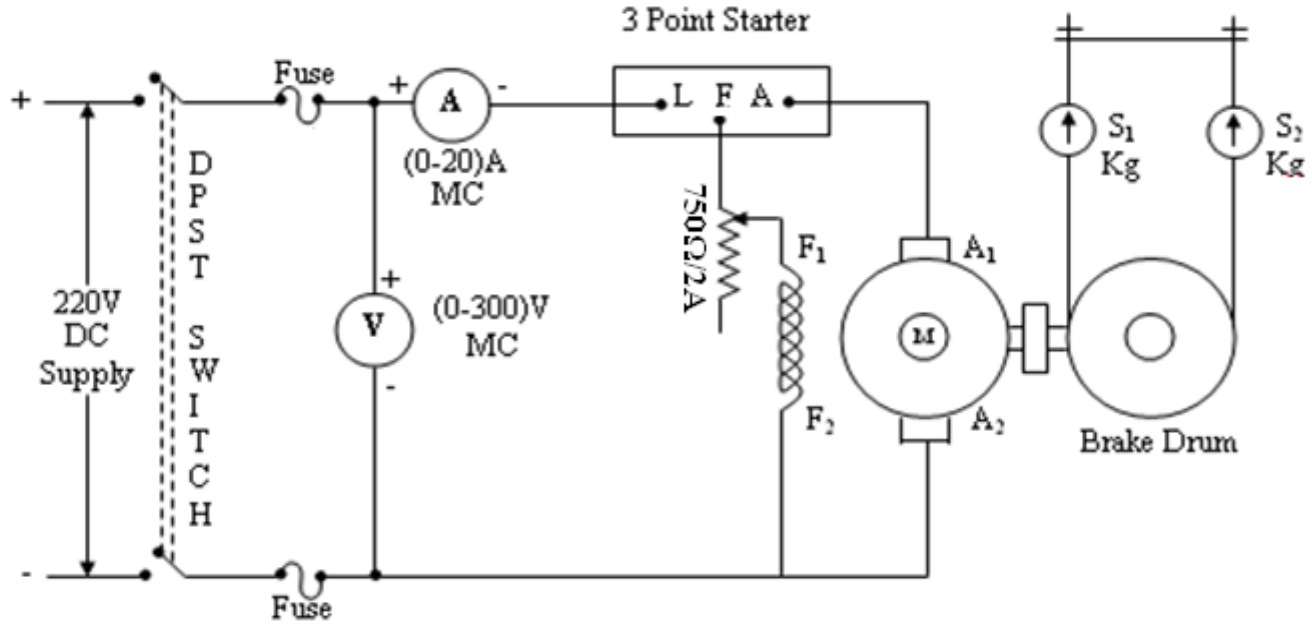
PROCEDURE:

1. Make the connections as per the circuit diagram
2. Switch on the power supply
3. Vary the RPS to a specified voltage and note down the corresponding ammeter readings
4. Repeat the above step for various RPS voltages and tabulate the readings

RESULT:

Thus, the Kirchoff's current law has been verified both theoretically and practically.

CIRCUIT DIAGRAM:



FUSE RATING:

125% of rated current

$$\frac{125 \times}{100} =$$

NAME PLATE DETAILS:

Rated Voltage :
Rated Current :
Rated Power :
Rated Speed :

Ex.No.

LOAD TEST ON DC SHUNT MOTOR

AIM:

To conduct load test on DC shunt motor and to find efficiency.

APPARATUS REQUIRED:

S.No.	Apparatus	Range	Type	Quantity
1	Ammeter	(0-20)A	MC	1
2	Voltmeter	(0-300)V	MC	1
3	Rheostat	750Ω, 2A	Wire Wound	1
4	Tachometer	(0-1500) rpm	Digital	1
5	Connecting Wires	2.5sq.mm.	Copper	Few

PRECAUTIONS:

1. DC shunt motor should be started and stopped under no load condition.
2. Field rheostat should be kept in the minimum position.
3. Brake drum should be cooled with water when it is under load.

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. After checking the no load condition, and minimum field rheostat position, DPST switch is closed and starter resistance is gradually removed.
3. The motor is brought to its rated speed by adjusting the field rheostat.
4. Ammeter, Voltmeter readings, speed and spring balance readings are noted under no load condition.
5. The load is then added to the motor gradually and for each load, voltmeter, ammeter, spring balance readings and speed of the motor are noted.
6. The motor is then brought to no load condition and field rheostat to minimum position, then DPST switch is opened.

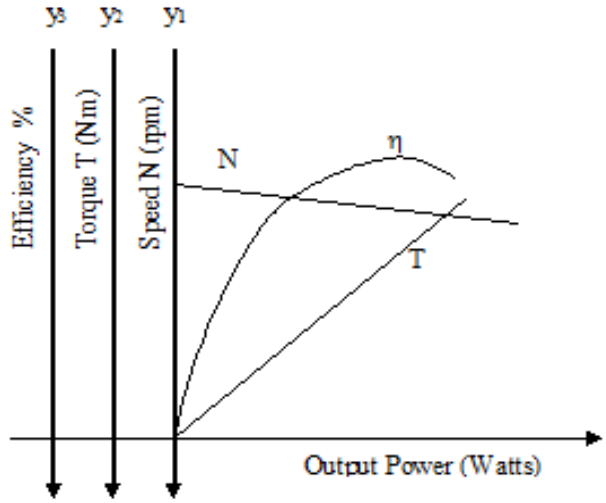
TABULAR COLUMN:

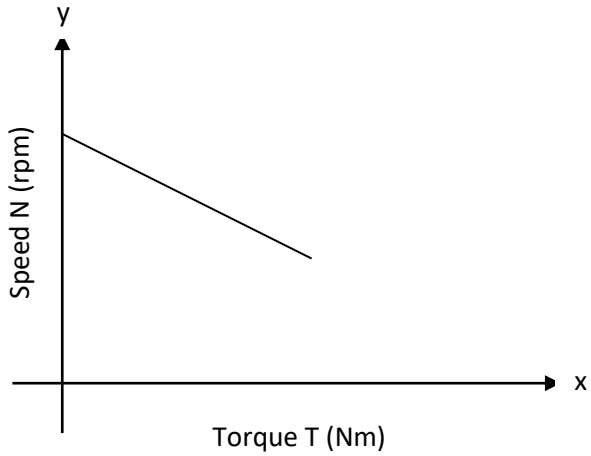
S.No.	Voltage V (Volts)	Current I (Amps)	Spring Balance Reading		$(S_1 \sim S_2)$Kg	Speed N (rpm)	Torque T (Nm)	Output Power Pm (Watts)	Input Power P_i (Watts)	Efficiency η%
			S_1(Kg)	S_2(Kg)						

Radius of the Brake drum = cm

Thickness of the Brake drum Belt = cm

MODEL GRAPHS:





FORMULAE:

Torque T = (S_1~ S_2) x (R+t/2) x 9.81 Nm

Input Power P_i = VI Watts

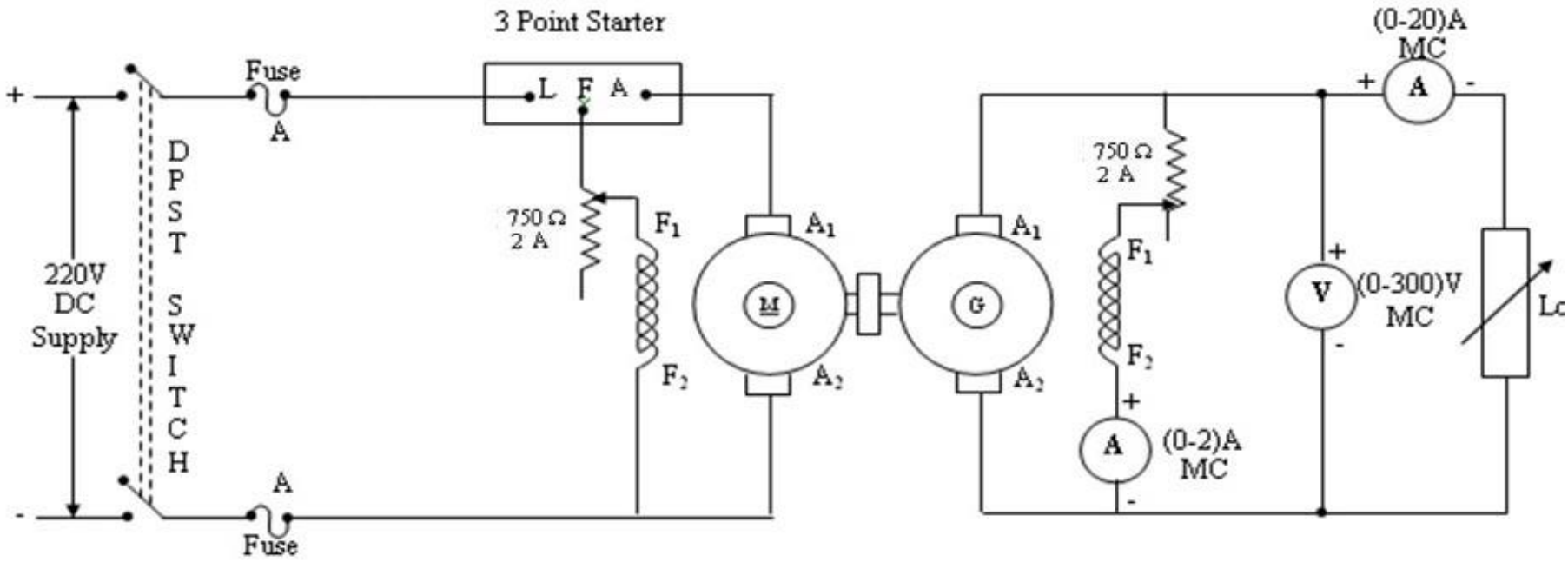
Output Power P_m = $\frac{2\pi NT}{60}$ Watts

Efficiency η % = $\frac{Output\ power}{Input\ power} \times 100\%$

RESULT:

Thus load test on DC shunt motor is conducted and its efficiency is determined.

CIRCUIT DIAGRAM:



FUSE RATING:

125% of rated current

$$\frac{125 \times \quad}{100} = \quad A$$

NAME PLATE DETAILS:

	Motor	Generator
Rated Voltage :	V	V
Rated Current :	A	A
Rated Power :	KW	KW
Rated Speed :	RPM	RPM

Ex.No.

LOAD TEST ON SELF EXCITED DC GENERATOR

AIM:

To conduct load test on self-excited DC shunt generator, to obtain its load characteristics of the machine

APPARATUS REQUIRED:

S.No.	Apparatus	Range	Type	Quantity
1	Ammeter	(0-5)A	MC	1
2	Voltmeter	(0-300)V	MC	1
3	Rheostats	750Ω, 2A	Wire Wound	2
4	SPST Switch	-	-	1
5	Tachometer	(0-1500)rpm	Digital	1
6	Connecting Wires	2.5sq.mm.	Copper	Few
7	Loading Rheostat	5KW, 230V	-	1

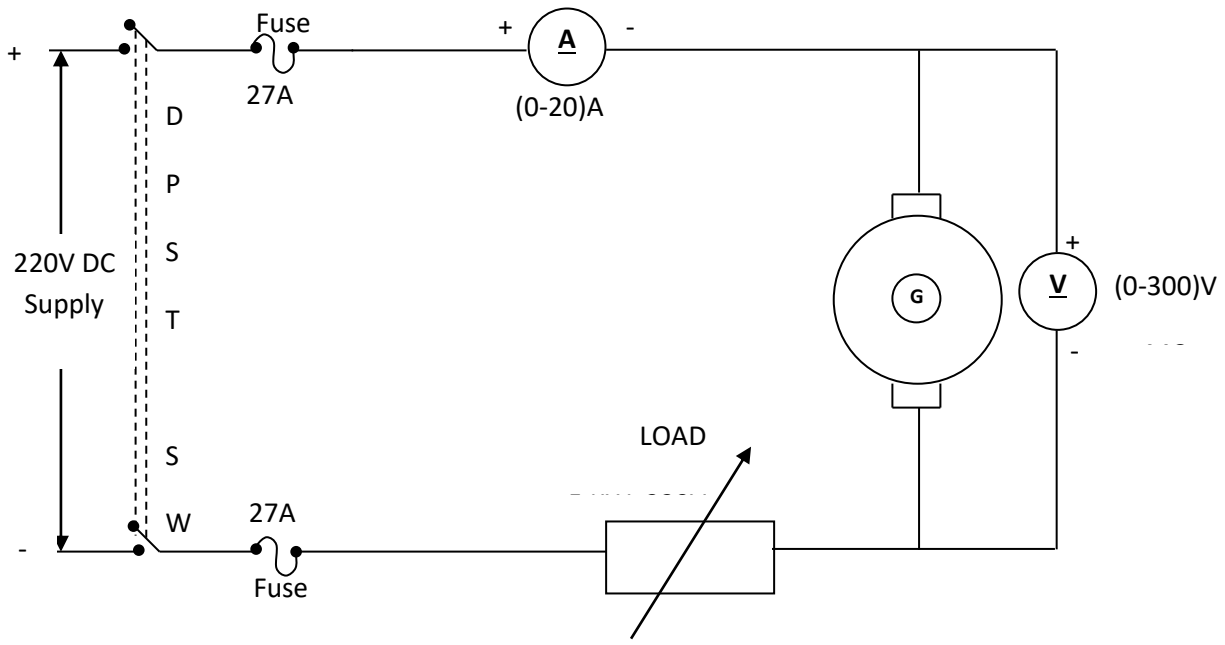
PRECAUTIONS:

1. The field rheostat of motor should be in minimum resistance position at the time of starting and stopping the machine.
2. The field rheostat of generator should be in maximum resistance position at the time of starting and stopping the machine.
3. SPST switch is kept open during starting and stopping.
4. No load should be connected to generator at the time of starting and stopping.

PROCEDURE: (LOAD TEST)

1. Connections are made as per the circuit diagram.

DETERMINATION OF ARMATURE RESISTANCE:



TABULAR COLUMN: (LOAD TEST)

S.No.	Field Current I_f (A)	Load Current I_L (A)	Terminal Voltage V (V)	Armature Current $I_a = I_L + I_f$ (A)	Generated emf $E_g = V + I_a R_a$ (V)

2. After checking minimum position of DC shunt motor field rheostat and maximum position of DC shunt generator field rheostat, DPST switch is closed and starting resistance is gradually removed.
3. Under no load condition, Ammeter and Voltmeter readings are noted, after bringing the voltage to rated voltage by adjusting the field rheostat of generator.
4. Load is varied gradually and for each load, voltmeter and ammeter readings are noted.
5. Then the generator is unloaded and the field rheostat of DC shunt generator is brought to maximum position and the field rheostat of DC shunt motor to minimum position, DPST switch is opened.

PROCEDURE: (R_a TEST)

1. Connections are made as per the circuit diagram.
2. Supply is given by closing the DPST switch.
3. Readings of Ammeter and Voltmeter are noted by varying the load in steps.
4. Armature resistance in Ohms is calculated as $R_a = (Vx1.5) /I$

FORMULAE:

$E_g = V + I_a R_a$ (V)

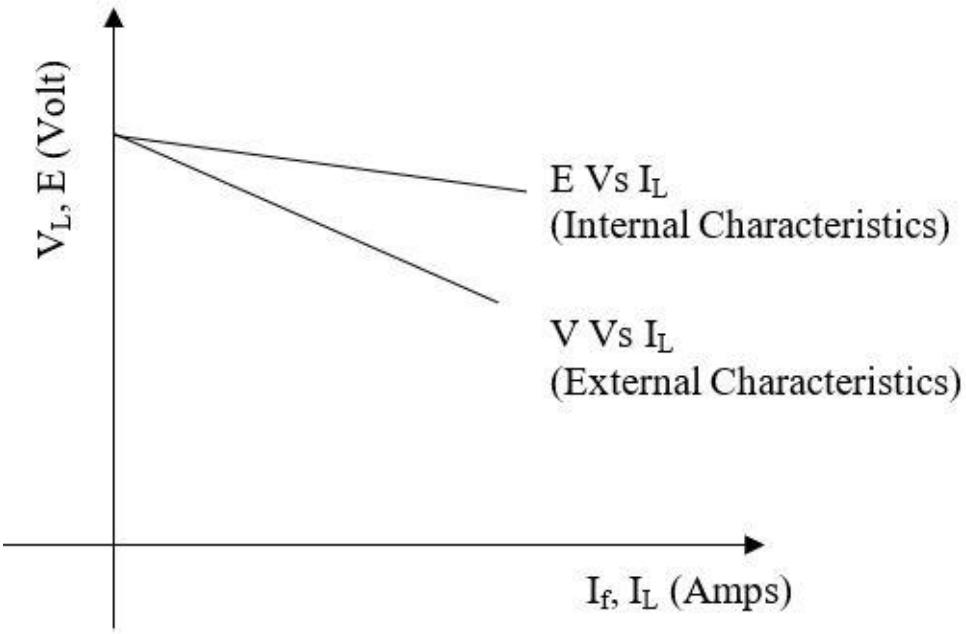
$I_a = I_L + I_f$ (A)

$R_a = (Vx1.5) /I$

TABULAR COLUMN: (R_a TEST)

S.No.	Voltage V (V)	Current I (A)	Armature Resistance R_a (Ohm)

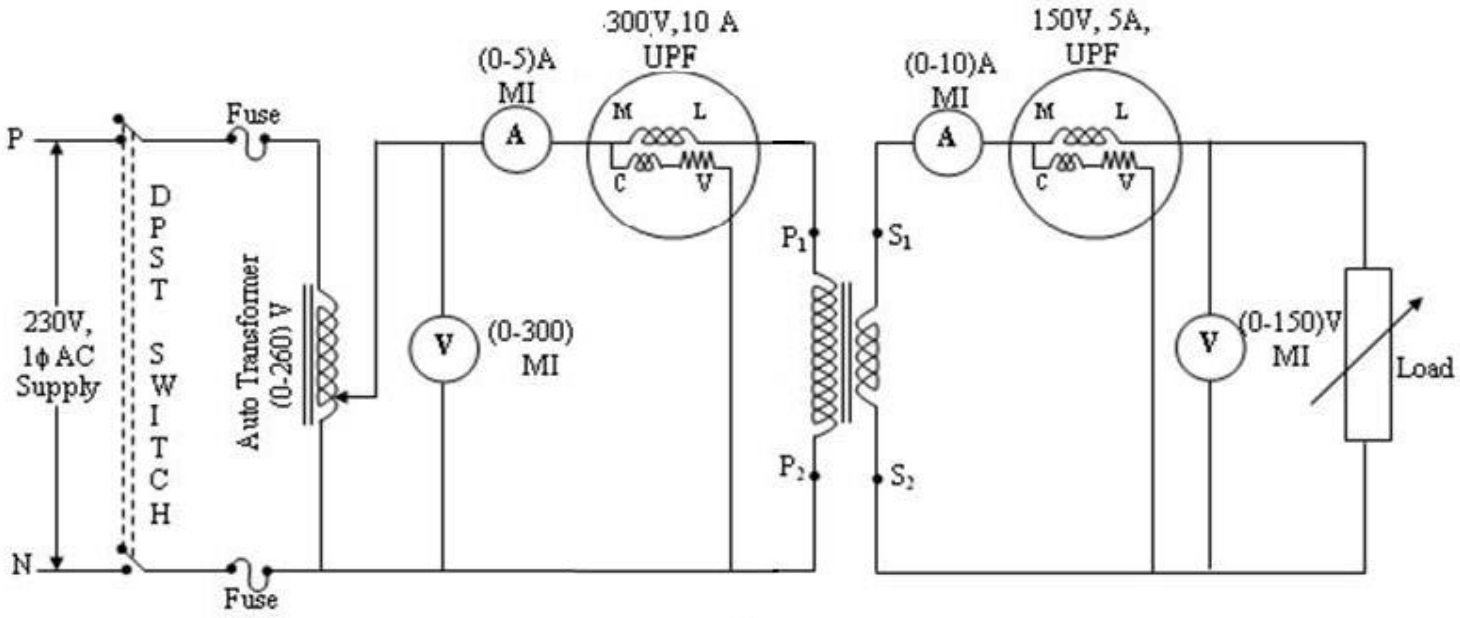
MODEL GRAPH:



RESULT:

Thus the open circuit test and load test on self-excited DC shunt generator are conducted and its open circuit characteristics and the load characteristics are obtained and its critical resistance is determined.

CIRCUIT DIAGRAM:



FUSE RATING:

125% of rated current

$$\frac{125 \times}{100} =$$

NAME PLATE DETAILS:

	Primary	**Secondary**
Rated Voltage :		
Rated Current :		
Rated Power :		

Ex.No.

LOAD TEST ON A SINGLE-PHASE TRANSFORMER

AIM:

To conduct load test on single phase transformer and to find efficiency and percentage regulation.

APPARATUS REQUIRED:

S.No.	Apparatus	Range	Type	Quantity
1	Ammeter	(0-10)A (0-5) A	MI MI	1 1
2	Voltmeter	(0-150)V (0-300) V	MI MI	1 1
3	Wattmeter	(300V, 5A) (150V, 5A)	Upf Upf	1 1
4	Auto Transformer	1ϕ, (0-260)V	-	1
5	Resistive Load	5KW, 230V	-	1
6	Connecting Wires	2.5sq.mm	Copper	Few

PRECAUTIONS:

1. Auto Transformer should be in minimum position.
2. The AC supply is given and removed from the transformer under no load condition.

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. After checking the no load condition, minimum position of auto transformer and DPST switch is closed.
3. Ammeter, Voltmeter and Wattmeter readings on both primary side and secondary side are noted.
4. The load is increased and for each load, Voltmeter, Ammeter and Wattmeter readings on both primary and secondary sides are noted.
5. Again no load condition is obtained and DPST switch is opened.

TABULAR COLUMN:

S. No.	Load	Primary		Secondary			Input Power W_1 x MF	Output Power W_2 x MF	Efficiency η %	% Regulation
		V_1 (Volts)	I_1 (Amps)	V_2 (Volts)	I_2 (Amps)	W_2 (Watts)				

FORMULAE:

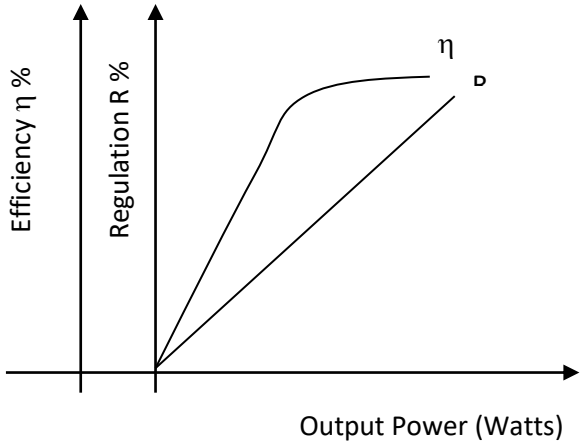
Output Power = W_2 x Multiplication factor

Input Power = W_1 x Multiplication factor

Efficiency η % $= \frac{Output\ power}{Input\ power} \times 100\%$

Regulation R % $= \frac{V_{NL} - V_{FL}}{V_{NL}} \times 100\%$

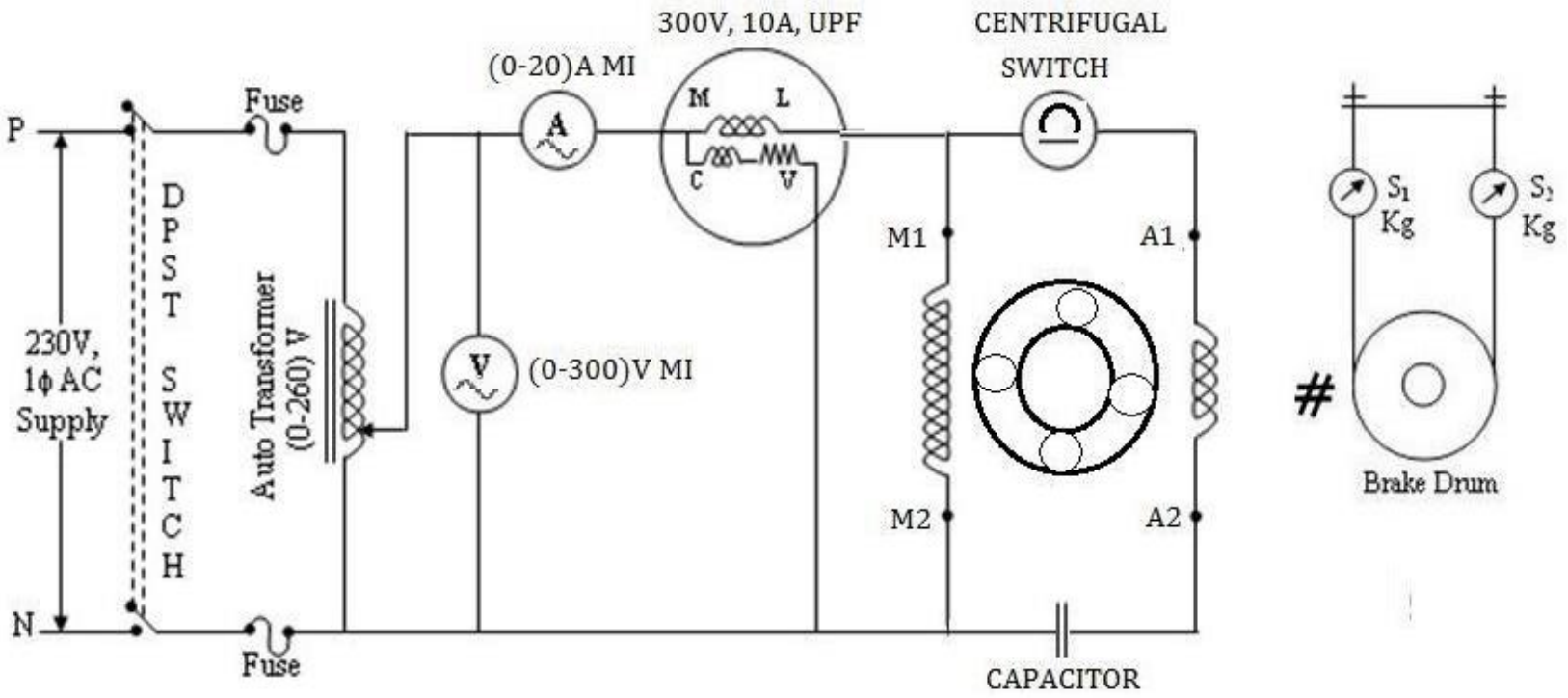
MODEL GRAPHS:



RESULT:

Thus the load test on single phase transformer is conducted.

CIRCUIT DIAGRAM



FUSE RATING:

125% of rated current

$$\frac{125 \times}{100} = \quad A$$

NAME PLATE DETAILS:

Motor

Rated Voltage : V
Rated Current : A
Rated Power : KW
Rated Speed : RPM

Ex.No.

LOAD TEST ON SINGLE PHASE INDUCTION MOTOR

AIM:

To predetermine performance characteristics of single phase induction motor and to plot the characteristic curves.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	TYPE	QTY
1	Wattmeter	600V,10A,UPF	M.C	1
2	Voltmeter	(0-300)V (0-600)V	M.C M.I	1 1
3	Ammeter	(0-10)A (0-2)A	M.I M.C	1 1
4	3φ Auto-transformer			

NAME PLATE DETAILS:

KW :
RPM :
Voltage :
Current :
Frequency :
Phase :

PRECAUTIONS:

To start and stop the machine

1. Keep the auto-transformer (at the input supply side) in its Minimum voltage position before starting the motor.
2. There should not be any load on the motor (loosen the belts on the brake drum)

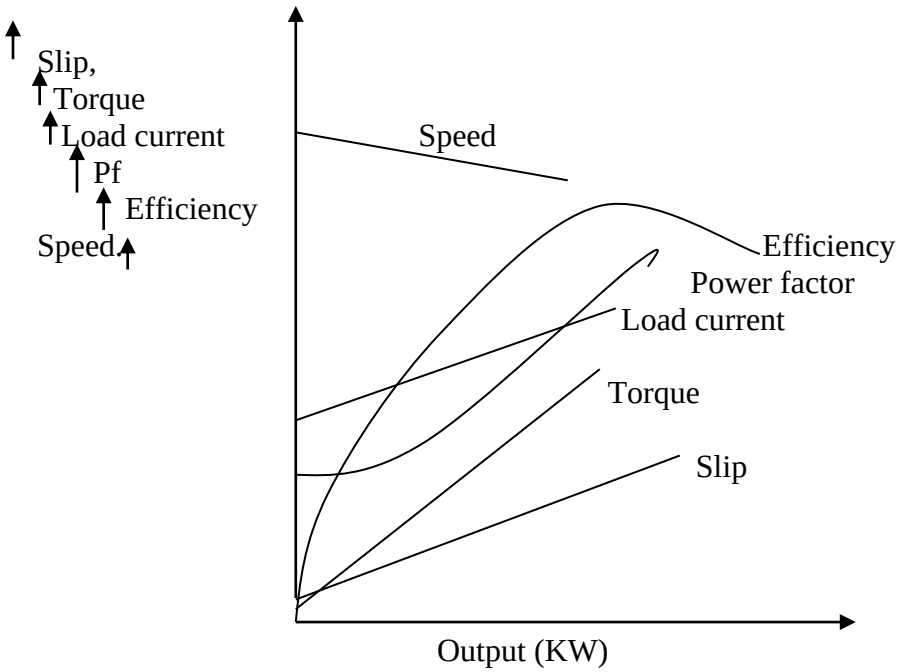
PROCEDURE:

1. The Circuit connections are given as per the Circuit diagram.
2. The input supply is increased until the motor runs at rated speed.

TABULAR COLUMN:

S.NO	I	V	SPRING BALANCE READING S1	S2	SPEED	WATT METER READINGS W1	W2	INPUT POWER	OUTPUT POWER	TORQUE	η	SLIP
	A	VOLT	KG	KG	RPM	WATTS	WATTS	WATTS	WATTS	NM	%	%

MODEL GRAPH:



3. Note down the no load readings for voltage, current, input power and speed.
4. Increase the no load torque by tightening the belt on the brake drum.
5. Note down the readings for voltmeter, wattmeter, spring balance, speed for different loads.

MODEL CALCULATION:

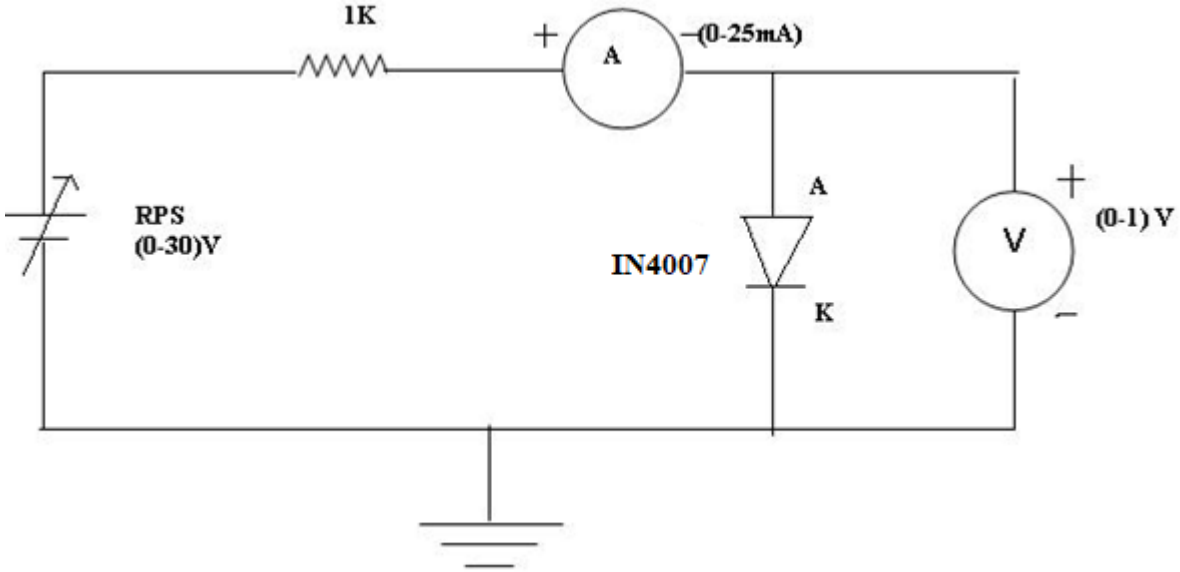
1. Torque T = (S_1~ S_2) x (R+t/2) x 9.81 Nm
2. Output Power P_m = $\frac{2\pi NT}{60}$ Watts
3. Efficiency η % = $\frac{Output\ power}{Input\ power} \times 100\%$
4. Power factor = $\frac{Input\ power}{\sqrt{3V_L I_L}}$
5. % Slip = $\frac{N_s - N}{N_s} \times 100$

RESULT:

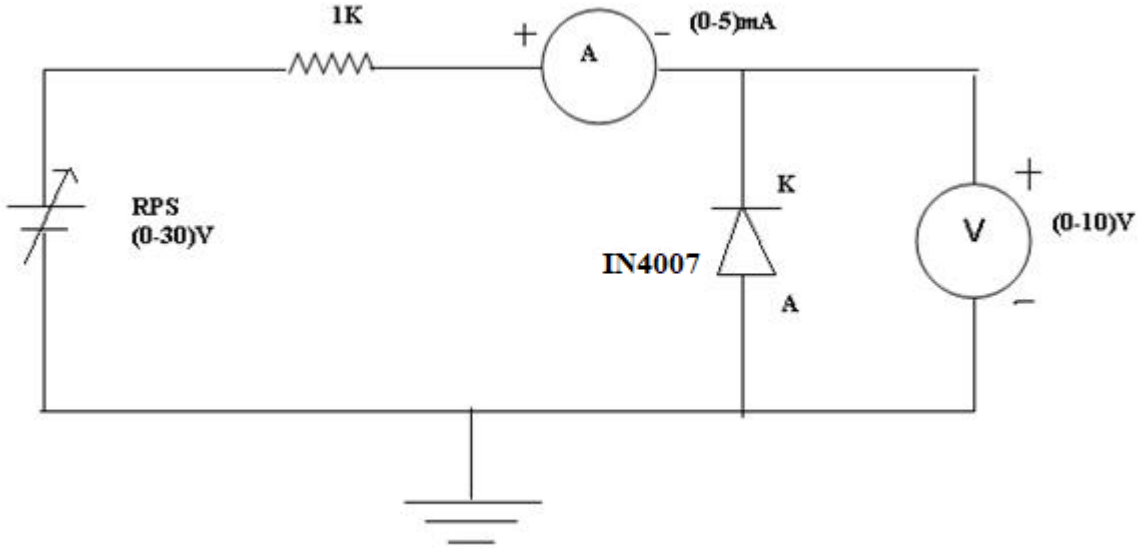
Thus the load test on single phase Induction motor was conducted and the performance characteristics were drawn.

CIRCUIT DIAGRAM:

FORWARD BIAS:



REVERSE BIAS:



Ex.no :

CHARACTERISTICS OF SEMICONDUCTOR (PN JUNCTION) DIODE

AIM:

To determine the VI characteristics of PN Diode

APPARATUS REQUIRED:

S.No	Name	Range	Type	Qty
1	R.P.S	(0-30)V		1
2	Ammeter	(0-100)μA, (0-25) mA		2 1
3	Voltmeter	(0-10)V (0-1)V		1 1
4	Connecting wires			
5	Bread Board			1
6	Resistors	1KΩ		2
7	Diode- PN	BY127		1

THEORY:

A diode is a PN junction formed by a layer of P type and layer of N type Semiconductors. Once formed the free electrons in the N region diffuse across the junction and combine with holes in P region and so a depletion Layer is developed. The depletion layer consists of ions, which acts like a barrier for diffusion of charged beyond a certain limit. The difference of potential across the depletion layer is called the barrier potential. At 2.5degree the barrier potential approximately equal 0.7v for silicon diode and 0.3v for germanium diode.

When the junction is forward bias, the majority carrier acquired sufficient energy to overcome the barrier and the diode conducts. When the junction is reverse biased the depletion layer widens and the barrier potential increases. Hence the Majority carrier cannot cross the junction and the diode does not conduct. But there will be a leakage current due to minority carrier. When diode is forward biased, resistance offered is zero, and when reverse biased resistance offered is infinity. It acts as a perfect switch.

TABULATION:

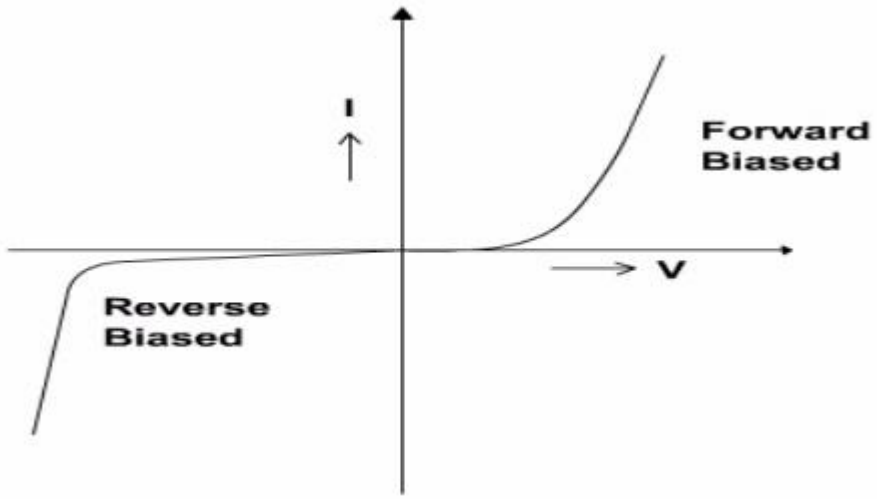
FORWARD BIAS:

V_f(volts)	I_f(mA)

REVERSE BIAS:

V_r(volts)	I_r(mA)

MODEL GRAPH



PROCEDURE:

FORWARD BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to anode of the diode and negative terminal to cathode of the diode.
3. Forward voltage V_f across the diode is increased in small steps and the forward current is noted.
4. The readings are tabulated. A graph is drawn between V_f and I_f.

REVERSEBIAS :

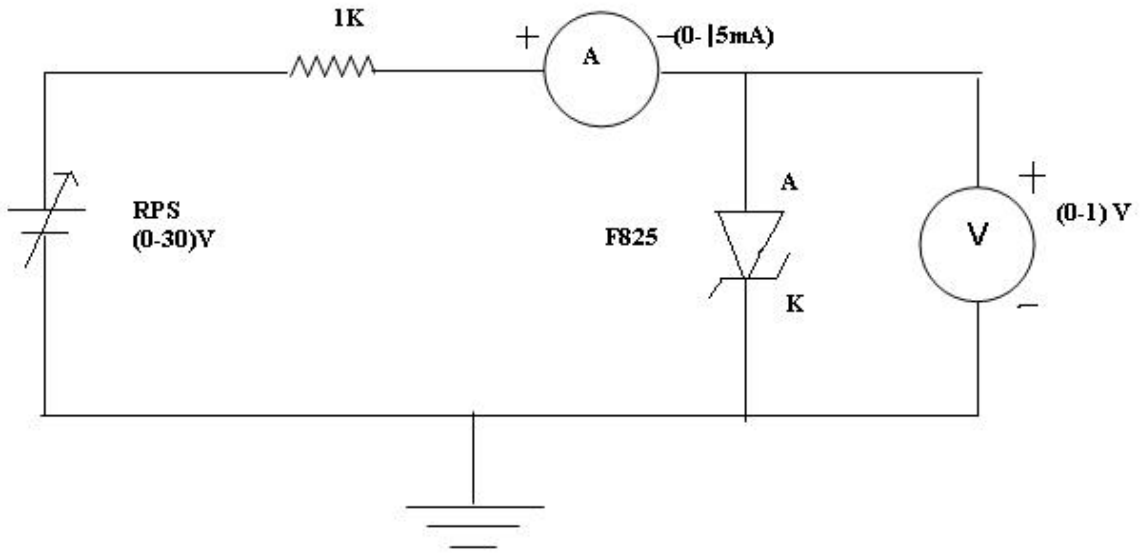
1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to cathode of the diode and negative terminal to anode of the diode.
3. Reverse voltage V_f across the diode is increased in small steps and the Reverse current is noted.

RESULT:

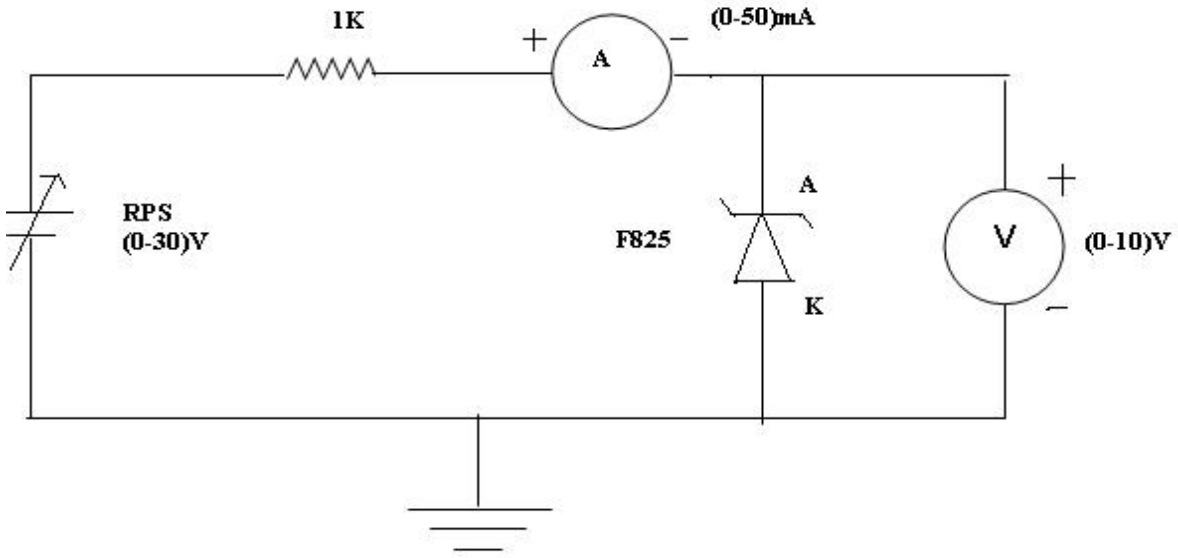
Thus the characteristics of PN-Junction diode were drawn**.**

CIRCUIT DIAGRAM:

FORWARD BIAS:



REVERSE BIAS:



Ex. No:

CHARACTERISTICS OF ZENER DIODE

AIM:

To determine the VI characteristics of Zener Diode

APPARATUS REQUIRED:

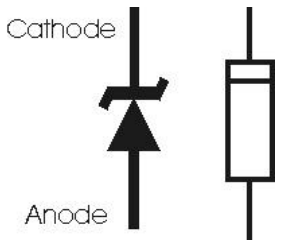
S.No	Name	Range	Type	Qty
1	R.P.S	(0-30)V		1
2	Ammeter	(0-15) mA (0-50) mA		1 1
3	Voltmeter	(0-10)V (0-1)V		1 1
4	Connecting wires			
5	Bread Board			1
6	Resistors	1KΩ		2
7	Diode- Zener	F825		1

THEORY:

Zener diodes have many of the same basic properties of ordinary semiconductor diodes. When forward biased,they conduct in the forward direction and have the same turn on voltage as ordinary diodes. For silicon this is about 0.6 volts.

In the reverse direction, the operation of a Zener diode is quite different to an ordinary diode. For low voltages the diodes do not conduct as would be expected. However, once a certain voltage is reached the diode "breaks down" and current flows. Looking at the curves for a Zener diode, it can be seen that the voltage is almost constant regardless of the current carried. This means that a Zener diode provides a stable and known reference voltage. Hence they are used as Voltage regulators.

PIN DIAGRAM:



TABULAR COLUMN:

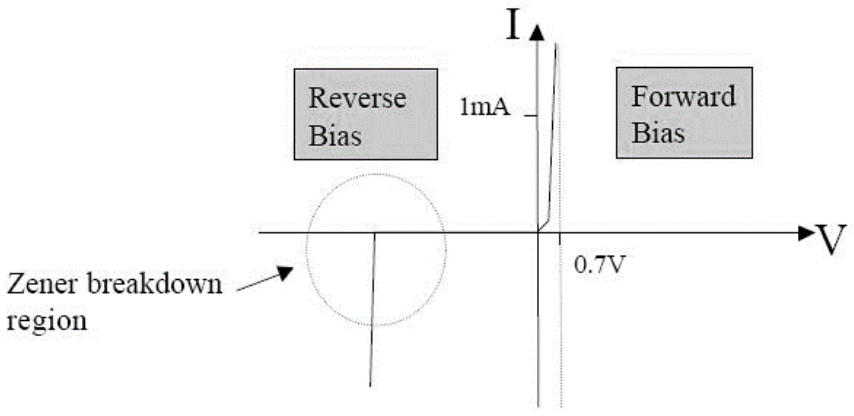
FORWARD BIAS:

V_f(volts)	I_f(mA)

REVERSE BIAS:

V_r(volts)	I_r(mA)

MODEL GRAPH



PROCEDURE:

FORWARD BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to anode of the diode and negative terminal to cathode of the diode.
3. Forward voltage V_f across the diode is increased in small steps and the forward current is noted.
4. The readings are tabulated. A graph is drawn between V_f and I_f.

REVERSEBIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to cathode of the diode and negative terminal to anode of the diode.
3. Reverse voltage V_f across the diode is increased in small steps and the Reverse current is noted.
4. The readings are tabulated. A graph is drawn between V_r and I_r.

REVIEW QUESTIONS:

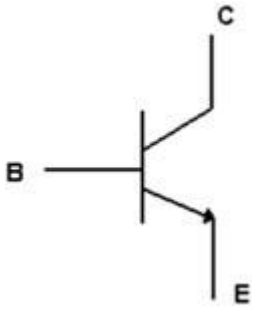
1. How Zener diode acts as a voltage regulator.
2. Explain working of a Zener Diode
3. What is the cut-in voltage of zener diode?
4. Differentiate between Zener Breakdown and Avalanche breakdown
5. Why zener diode is often preferred than PN diode
6. List the application of zener diode
7. Define zener breakdown voltage
8. Define Zener diode

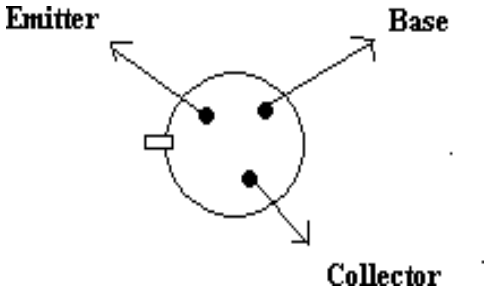
RESULT:

Thus the characteristics of Zener diode were drawn**.**

COMMON EMITTER INPUT-OUTPUT CHARACTERISTICS

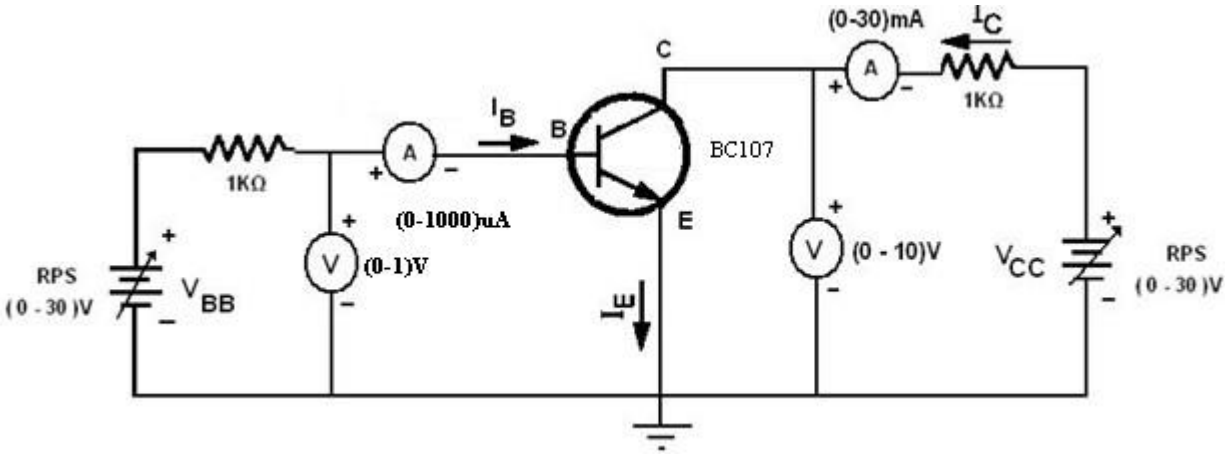
SYMBOL:(NPN TRANSISTOR)) **PIN DIAGRAM: (BOTTOM VIEW**



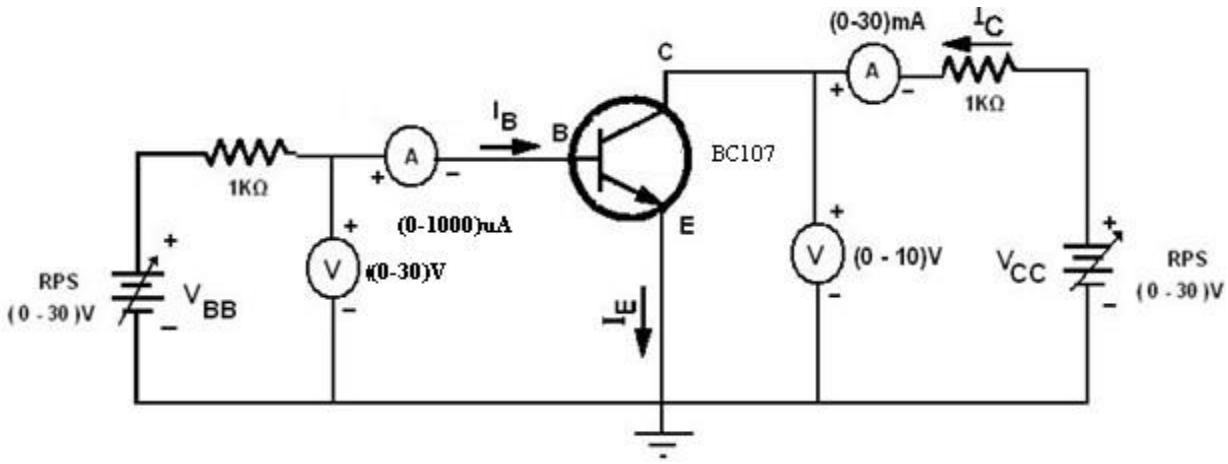


CIRCUIT DIAGRAM:

INPUT CHARACTERISTICS



OUTPUT CHARACTERISTICS



Ex .No.

CHARACTERISTICS OF BJT

AIM:

- To draw the input and output characteristics of transistor connected in CE configuration
- To find β of the given transistor and also its h parameters.

APPARATUS REQUIRED:

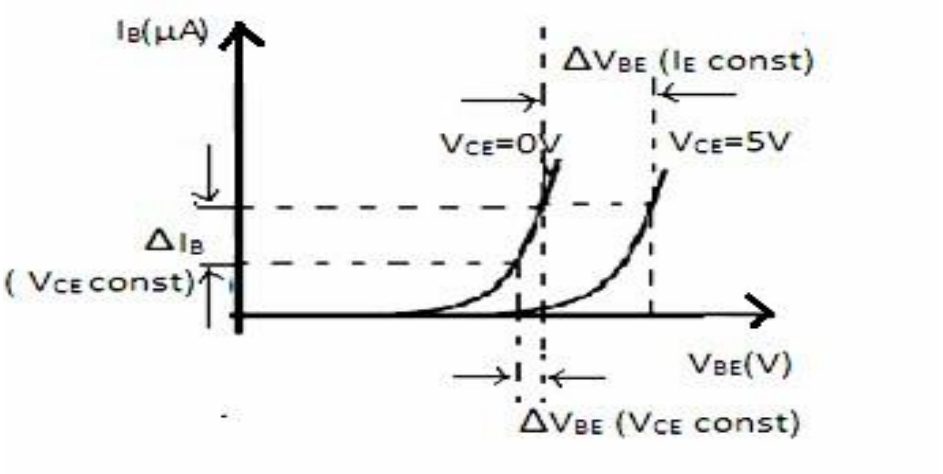
S.No.	Name of the apparatus	Range	Quantity
1.	Transistor	BC107	1No
2.	Dual Regulated Power supply	(0-30V)	1No
3.	Resistor	1KΩ	1No
4.	Ammeter	(0-30 mA)	1No
5.	Ammeter	(0-1000μA)	1No
6.	Voltmeters	(0-20V) , (0-1)V, (0-10)V	Each 1No
7.	Bread board	-	1 No
8.	Connecting wires	Single strand	As required

THEORY:

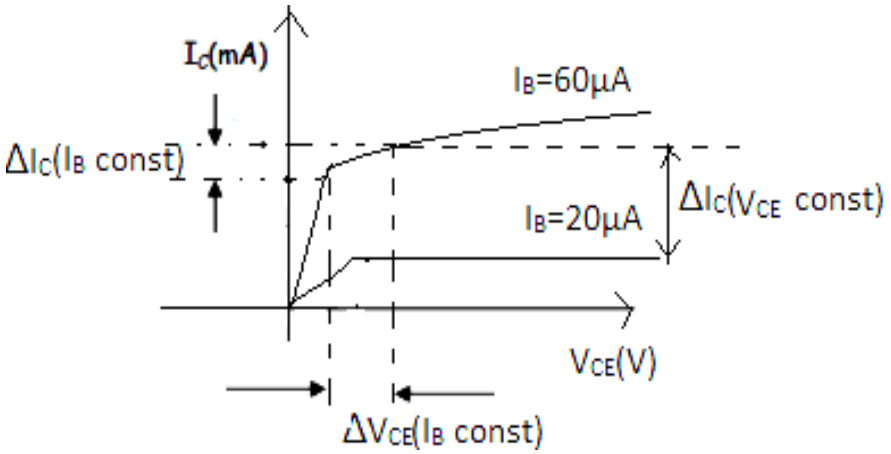
In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. Therefore the emitter terminal is common to both input and output. The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement IB increases less rapidly with VBE. Therefore input resistance of CE circuit is higher than that of CB circuit. The output characteristics are drawn between Ic and VCE at constant IB. the collector current varies with VCE up to few volts only. After this the collector current becomes almost constant, and independent of VCE. The value of VCE up to which the collector current changes with V CE is known as Knee voltage.

MODEL GRAPH:

A) INPUT CHARACTERISTICS:



A) OUTPUT CHARACTERSITICS:



Calculations:

1. **Input Characteristics:** To obtain input resistance find ΔV_{BE} and ΔI_B for a constant $\mathbf{V_{CE}}$ on one of the input characteristics.
   Input impedance = $\mathbf{h_{ie}= R_i}$ = $\mathbf{\Delta V_{BE}/ \Delta I_B}$($\mathbf{V_{CE}}$is constant)Reverse voltage gain = $\mathbf{h_{re}= \Delta V_{EB}/ \Delta V_{CE}}$($\mathbf{I_B}$= constant)
2. **Output Characteristics:** To obtain output resistance find $\mathbf{\Delta I_C}$and $\mathbf{\Delta V_{CB}}$at aconstant $\mathbf{I_B}$.Output admittance **1/hoe** = $\mathbf{R_o}$ = $\mathbf{\Delta I_C/ \Delta V_{CE}}$($I_B$is constant)
   Forward current gain = $\mathbf{h_{fe}}$ = $\mathbf{\Delta I_C/ \Delta I_B}$($\mathbf{V_{CE}}$= constant)
3. Current amplification factor β = ΔIC/ΔIB

PROCEDURE:

A) INPUT CHARACTERISTICS

1. Connect the circuit as per the circuit diagram.
2. For plotting the input characteristics the output voltage VCE is kept constant at 1V and fordifferent values of VBB , note down the values of IB and VBE
3. Repeat the above step by keeping VCE at 2V and 4V and tabulate all the readings.
4. Plot the graph between VBE and IB for constant VCE

B) OUTPUT CHARACTERISTICS:

1. Connect the circuit as per the circuit diagram
2. For plotting the output characteristics the input current IB is kept constant at 50μA and fordifferent values of VCC note down the values of IC and VCE
3. Repeat the above step by keeping IB at 75 μA and 100 μA and tabulate the all the readings
4. Plot the graph between VCE and IC for constant IB

PRECAUTIONS:

1. The supply voltage should not exceed the rating of the transistor
2. Meters should be connected properly according to their polarities

TABULATION:

Input Characteristics				
V_{BB} (Volts)	V_{CE} = 0V		V_{CE} = 5V	
	V_{BE} (Volts)	I_B (µA)	V_{BE} (Volts)	I_B (µA)

Output Characteristics						
VCC (Volts)	IB = 0 µA		IB = 20 µA		IB = 40 µA	
	VCE (Volts)	IC (mA)	VCE (Volts)	IC (mA)	VCE (Volts)	IC (mA)

RESULT:

Thus obtained the input and output characteristics of transistor connected in CE configuration and determined its parameters as follows.

Input impedance = $\mathbf{h_{ie}= R_i}$ =

Reverse voltage gain **=** $\mathbf{h_{re}=}$

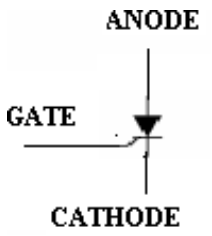
Output admittance **1/hoe** = $\mathbf{R_o}$ =

Forward current gain = $\mathbf{h_{fe}}$ =

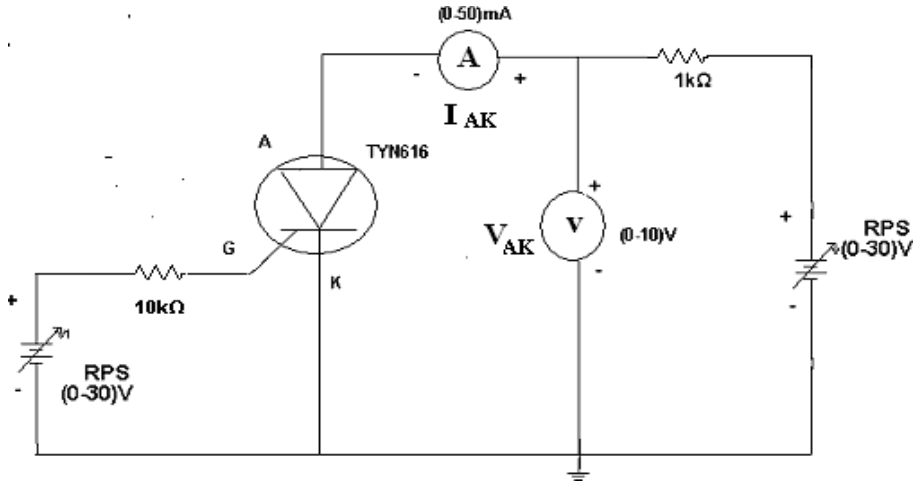
Current amplification factor β =

SCR CHARACTERISTICS

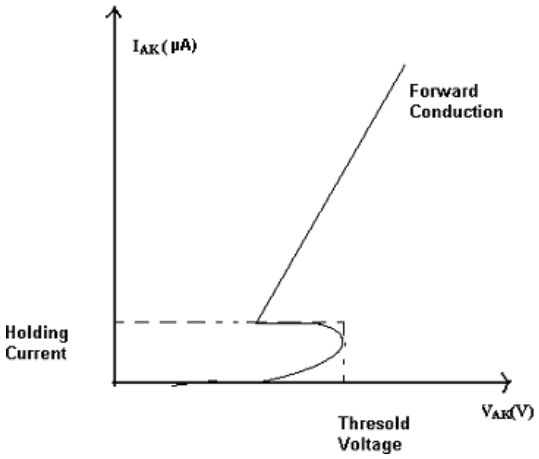
SYMBOL



CIRCUIT DIAGRAM:



V-I CHARACTERISTICS:



Ex.No CHARACTERISTICS OF SCR (SILICON-CONTROLLED RECTIFIER)

AIM:

To obtain the V-I Characteristics of SCR and also to determine the break over voltage and holdingcurrent.

APPARATUS REQUIRED:

S.No.	Name of the apparatus	Range	Quantity
1.	SCR	TYN616	1No
2.	Dual Regulated Power supply	(0-30V)	1No
3.	Resistor	10KΩ,1KΩ	Each 1
4.	Ammeters	(0-50) mA	1No
5.	Voltmeters	(0-10V)	1No
6.	Bread board	-	1 No
7.	Connecting wires	Single strand	As required

THEORY:

It is a four layer semiconductor device being alternate of P-type and N-type silicon. It consists of 3 junctions J1, J2, J3 the J1 and J3 operate in forward direction and J2 operates in reverse direction and three terminals called anode A, cathode K , and a gate G. The operation of SCR can be studied when the gate is open and when the gate is positive with respect to cathode. When gate is open, no voltage is applied at the gate due to reverse bias of the junction J2 no current flows through R2 and hence SCR is at cut off. When anode voltage is increased J2 tends to breakdown. When the gate positive, with respect to cathode J3 junction is forward biased and J2 is reverse biased .Electrons from N-type material move across junction J3 towards gate while holes from P-type material moves across junction J3 towards cathode. So gate current starts flowing, anode current increase is in extremely small current junction J2 break down and SCR conducts heavily. When gate is open thee break over voltage is determined on the minimum forward voltage at which SCR conducts heavily. Now most of the supply voltage appears across the load resistance. The holding current is the maximum anode current gate being open, when break over occurs.

OBSERVATION:

VAK(V)	IAK (μA)

PROCEDURE:

1. Connections are made as per circuit diagram.
2. Keep the gate supply voltage at some constant value
3. Vary the anode to cathode supply voltage and note down the readings of voltmeter and ammeter.Keep the gate voltage at standard value.
4. A graph is drawn between VAK and IAK.
5. From the graph note down the threshold voltage and Holding current values.

CALCULATIONS:

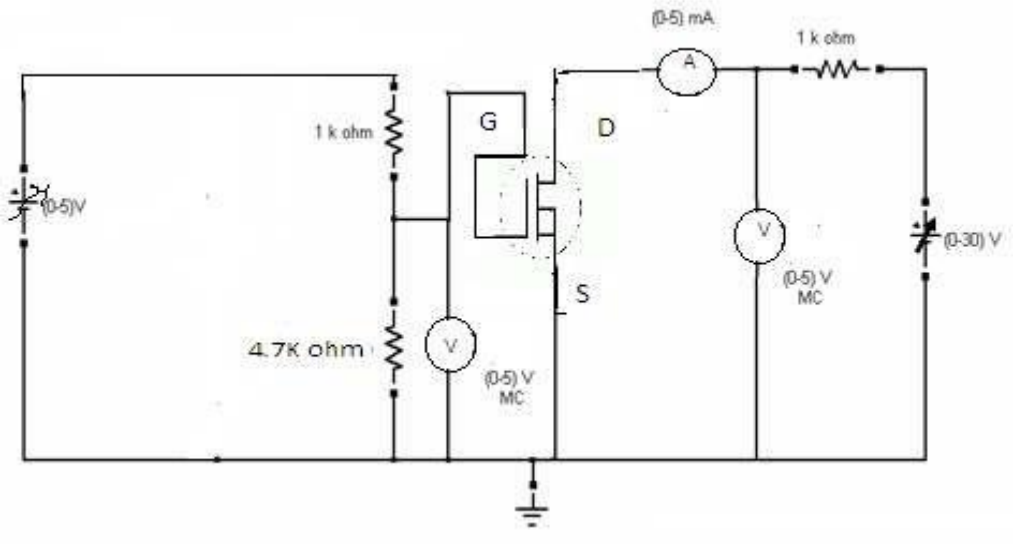
Threshold Voltage =

Holding Current =

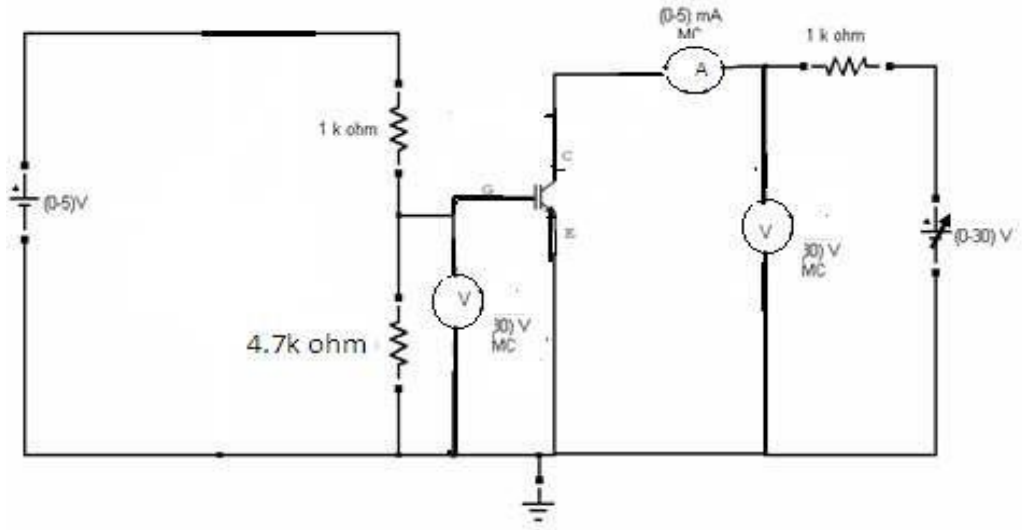
RESULT:

The V-I Characteristics of the SCR have been plotted.

CIRCUIT DIAGRAM (MOSFET):



CIRCUIT DIAGRAM (IGBT) :



Ex.No. **CHARACTERISTICS OF MOSFET**

AIM:

To determine the characteristics of MOSFET

A**PPARATUS REQUIRED**:

S.No.	APPARATUS	RANGE	TYPE	QUANTITY
1	MOSFET Module kit	220 V / 5 A		1
2	Regulated Power Supply	(0-15) V		1
3	Regulated Power Supply	(0-30) V		1
4	Voltmeter	(0-5) V	MC	1
5	Voltmeter	(0-30) V	MC	1
6	Ammeter	(0-5) mA	MC	1
7	Resistor	4.7 KΩ, 1 kΩ		1
8	Patch Chords			10

PROCEDURE:

1) Make the connections as per the circuit diagram.
2) Switch on the supply.
3) Set the gate current at a fixed value by varying RPS on the gate-cathode side.
4) Vary the voltage applied across Gate and corresponding V_{DS} (V_{CE}) and I_D(I_C) is noted.
5) The above steps are repeated for different values of I_G.
6) Vary the voltage across Collector and Emitter and noted down V_{GE} and I_C.
7) Draw the graph between V_{GS}(V_{CE})and I_D(I_C) and V_{GS}(V_{GE})and I_D(I_C).

TABULAR COLUMN (MOSFET):

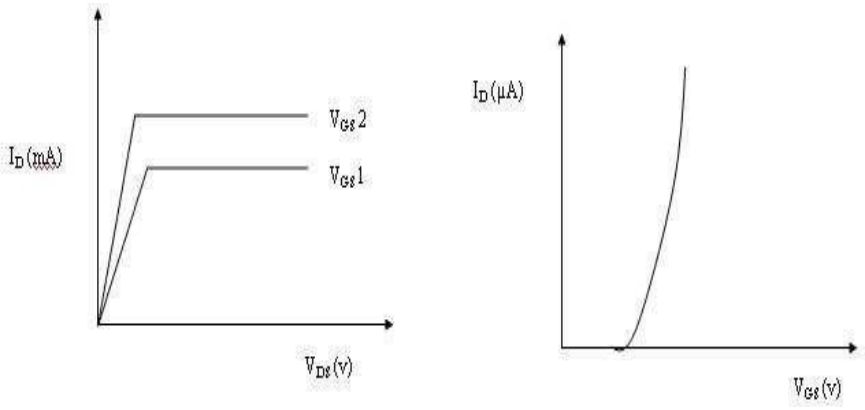
DRAIN CHARACTERISTICS:

S.No	V_{GS} =….(V)		V_{GS} =….(V)	
	V_{DS} (mV)	I_D (mA)	V_{DS} (mV)	I_D (mA)

TRANSFER CHARACTERISTICS:

S.No	V_{DS} =….(V)	
	V_{GS} (mV)	I_D (mA)

MODEL GRAPH



RESULT:

Thus the Characteristics of MOSFET were obtained.

3. Note down the no load readings for voltage, current, input power and speed.
4. Increase the no load torque by tightening the belt on the brake drum.
5. Note down the readings for voltmeter, wattmeter, spring balance, speed for different loads.

MODEL CALCULATION:

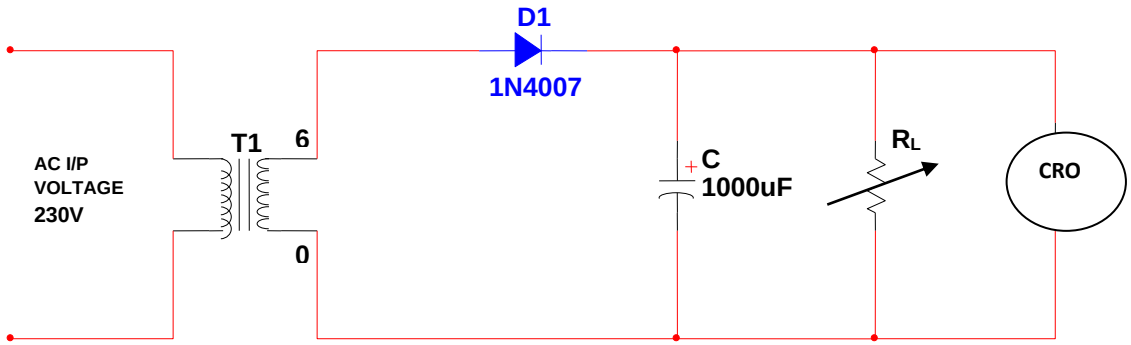
1. Torque T = (S_1~ S_2) x (R+t/2) x 9.81 Nm
2. Output Power P_m = $\frac{2\pi NT}{60}$ Watts
3. Efficiency η % = $\frac{Output\ power}{Input\ power} \times 100\%$
4. Power factor = $\frac{Input\ power}{\sqrt{3V_L I_L}}$
5. % Slip = $\frac{N_s - N}{N_s} \times 100$

RESULT:

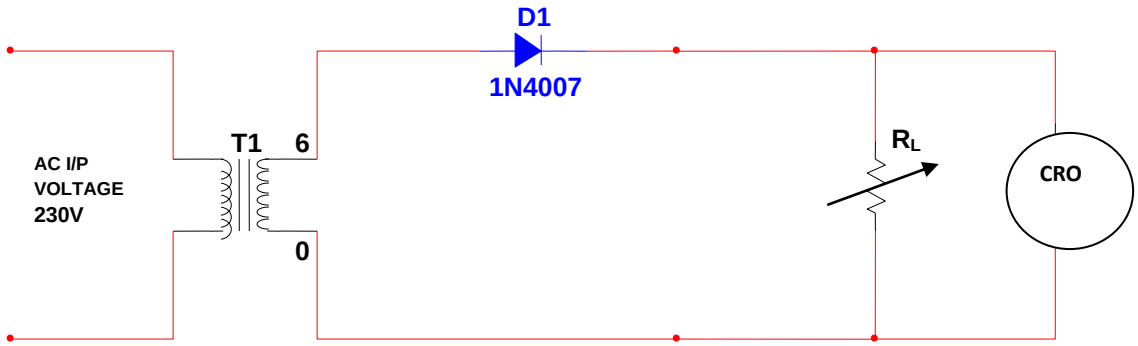
Thus the load test on single phase Induction motor was conducted and the performance characteristics were drawn.

CIRCUIT DIAGRAM:

WITH FILTER:



WITHOUT FILTER:



TABULAR COLUMN:

WITHOUT FILTER: T=

S.No	$R_L(\Omega)$	V_m (volts)	$V_{rms} = \frac{V_m}{2}$	$V_{dc} = \frac{V_m}{\pi}$	$I_{dc} = \frac{V_{dc}}{R_L}$	$\gamma = \sqrt{\frac{(V_{rms})^2}{(V_{dc})^2} - 1}$

Ex. No.

HALF WAVE RECTIFIER

AIM:

1. To design a half wave rectifier with and without simple capacitor filter.
2. Measurement of DC voltage under load and ripple factor, comparison with calculated values.

APPARATUS REQUIRED:

S.NO	COMPONENT	RANGE	QUANTITY
1	Center Tapped Transformer	6-0-6	1
2	Diode	1N4007	1
3	Capacitor	1000μF	1
4	CRO	(0-30)MHz	1
5	DRB		1

FORMULA USED:

WITHOUT FILTER, $\gamma = \sqrt{\frac{(V_{rms})^2}{(V_{dc})^2} - 1}$

WITH FILTER, $\gamma = \frac{V_{rms}}{V_{dc}}$

DESIGN:

Ripple factor with filter, $\gamma = \frac{1}{2\sqrt{3f} * C * R_L}$

Ripple factor without filter, $\gamma = \sqrt{\frac{(V_{rms})^2}{(V_{dc})^2} - 1}$ where $V_{rms} = \frac{V_m}{2}$, $V_{dc} = \frac{V_m}{\pi}$

$$\gamma = \sqrt{\frac{(\frac{V_m}{2})^2}{(\frac{V_m}{\pi})^2} - 1} = \sqrt{\frac{(\pi)^2}{4} - 1} = \sqrt{1.4674} = 1.211$$

THEORY:

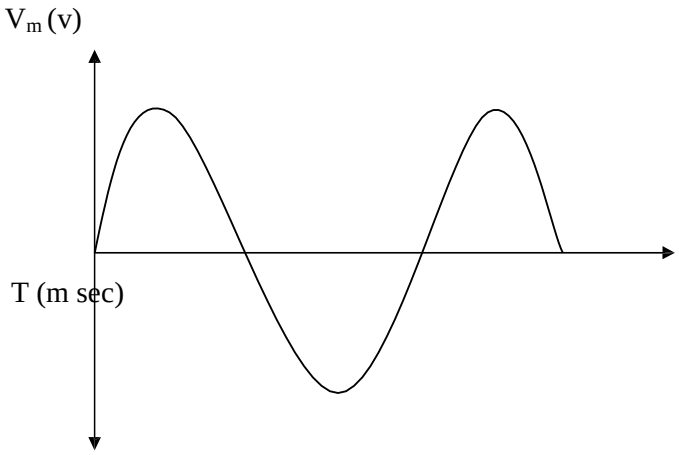
It converts an ac voltage into pulsating dc voltage using only one half of the applied ac voltage. The rectifying diode conducts during one half of the ac cycle only.

During the positive half of the cycle the input signal, the anode of the diode becomes positive with respect to the cathode and hence the diode conducts.

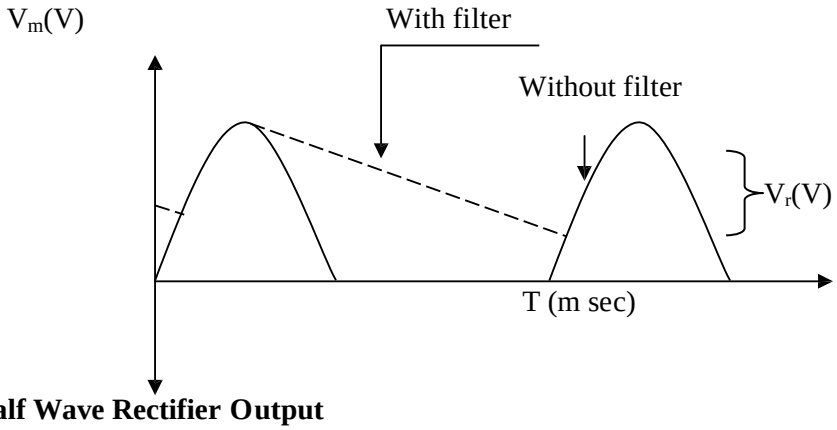
WITH FILTER: **T=** **T_R=** **T_F =**

S.No	$R_L(\Omega)$	V_m (volts)	V_r (volts)	$V_{rms} = \frac{V_r}{\sqrt{3}}$	$V_{dc} = V_m - \frac{V_r}{2}$	$I_{dc} = \frac{V_{dc}}{R_L}$	$\gamma = \frac{V_{rms}}{V_{dc}}$

MODEL GRAPH:



Input Waveform



Half Wave Rectifier Output

During the negative half of the cycle of the input signal, of the anode of the diode becomes negative with respect to the cathode and hence the diode does not conduct.

Output voltage is seen for positive Half of input only. Output Of rectifier is pulsating DC (With ripples) and remove them, C filter is connected parallel with load which bypasses AC components to ground.

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. Output waveform in CRO is observed, Amplitude, Time period is noted.
3. A capacitor is inserted in parallel to load resistor R_L which acts as filter section.
4. The output waveform with filter obtained in CRO is observed, the amplitude and the time period are noted and the graph is plotted.

The zener diode is connected in parallel with the load and determines the load regulation characteristics.

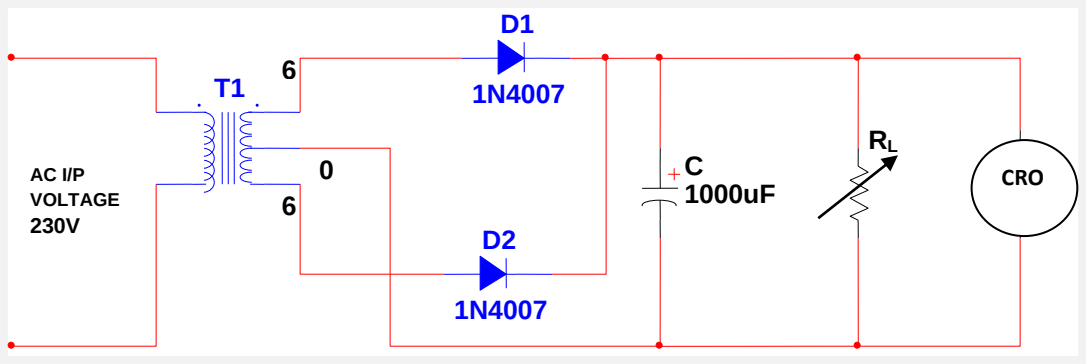
RESULT:

Thus the half wave rectifier is designed with and without capacitor filter and the corresponding dc output voltages and the ripple factors are measured and verified with thetheoretical values.

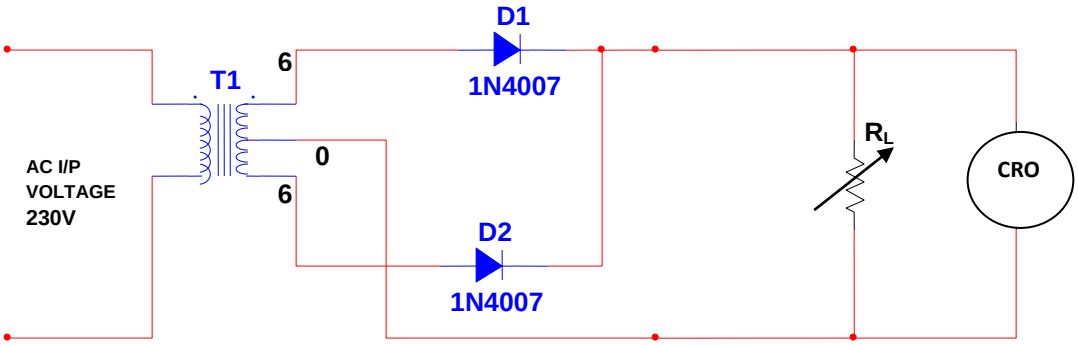
RIPPLE FACTOR		
	THEORETICAL	**PRACTICAL**
WITH FILTER		
WITH OUT FILTER		

CIRCUIT DIAGRAM:

WITH FILTER:



WITHOUT FILTER:



TABULAR COLUMN:

WITHOUT FILTER: T=

S.No	$R_L(\Omega)$	V_m (volts)	$V_{rms} = \frac{V_m}{\sqrt{2}}$	$V_{dc} = \frac{2V_m}{\pi}$	$I_{dc} = \frac{V_{dc}}{R_L}$	$\gamma = \sqrt{\frac{(V_{rms})^2}{(V_{dc})^2} - 1}$

Ex. No.

FULL WAVE RECTIFIER

AIM:

1. To designn a full wave rectifier with and without simple capacitor filter.
2. Measurement of DC voltage under load and ripple factor, comparison with calculated values.
3. Plot the load regulation characteristics using zener diode.

APPARATUS REQUIRED:

S.NO	COMPONENT	RANGE	QUANTITY
1	Center Tapped Transformer	6-0-6	1
2	Diode	1N4007	2
3	Capacitor	1000μF	1
4	CRO	(0-30)MHz	1
5	DRB		1
6	Voltmeter	(0-10)V	1
7	Ammeter	(0-10)mA	1
8	Zener Diode	1Z5.6	1
9	Resistor	1KΩ	1

FORMULA USED:

WITHOUT FILTER, $\gamma = \sqrt{\frac{(V_{rms})^2}{(V_{dc})^2} - 1}$

WITH FILTER, $\gamma = \frac{V_{rms}}{V_{dc}}$

DESIGN:

Ripple factor with filter, $\gamma = \frac{1}{4\sqrt{3f} * C * R_L}$

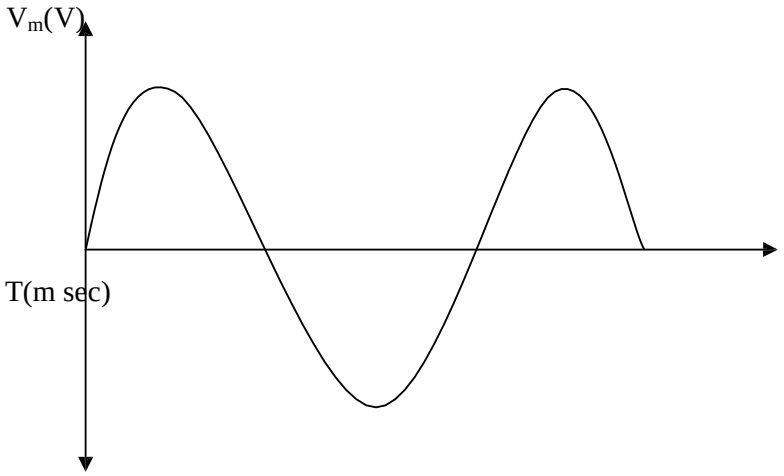
Ripple factor without filter, $\gamma = \sqrt{\frac{(V_{rms})^2}{(V_{dc})^2} - 1}$ where $V_{rms} = \frac{V_m}{\sqrt{2}}$, $V_{dc} = \frac{2V_m}{\pi}$

$$\gamma = \sqrt{\frac{(\frac{V_m}{\sqrt{2}})^2}{(\frac{2V_m}{\pi})^2} - 1} = \sqrt{\frac{(\pi)^2}{8} - 1} = \sqrt{0.23245} = 0.48$$

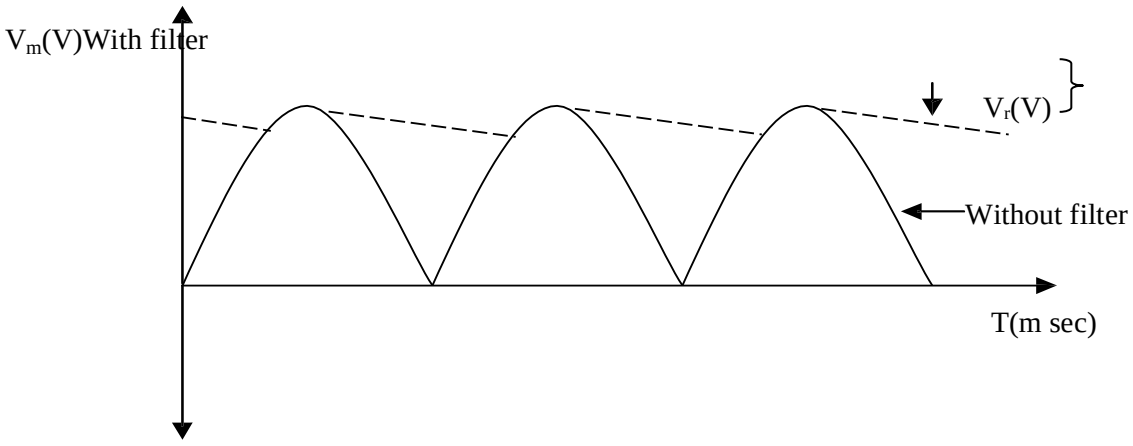
WITH FILTER: **T=** **T_R=** **T_F =**

S.No	$R_L(\Omega)$	V_m (volts)	V_r (volts)	$V_{rms} = \frac{V_r}{2\sqrt{3}}$	$V_{dc} = V_m - \frac{V_r}{2}$	$I_{dc} = \frac{V_{dc}}{R_L}$	$\gamma = \frac{V_{rms}}{V_{dc}}$

MODEL GRAPH:



Input Waveform



Full Wave Rectifier Output

THEORY:

The Full wave rectifier conducts for both the positive and negative half cycles of the input ac supply. In order to rectify both the half cycles of the ac input, two diodes are used in this circuit. The diode feed a common load R_L with the help of a centre tapped transformer. The ac voltage is applied through a suitable power transformer with proper turn's ratio. The rectifier's dc output is obtained across the load.

The dc load current for the full wave rectifier is twice that of the half wave rectifier. The lowest ripple factor is twice that of the full wave rectifier. The efficiency of full wave rectifier is twice that of full wave rectifier. The ripple factor also for the full wave rectifier is less compared to the half wave rectifier.

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. Output waveform in CRO is observed, Amplitude, Time period is noted.
3. A capacitor is inserted in parallel to load resistor R_L which acts as filter section.
4. The output waveform with filter obtained in CRO is observed, the amplitude and the time period are noted and the graph is plotted.
5. The zener diode is connected in parallel with the load and determines the load regulation characteristics.

RIPPLE FACTOR		
	THEORETICAL	**PRACTICAL**
WITH FILTER		
WITH OUT FILTER		

RESULT:

Thus the Full Wave Rectifier is designed with and without capacitor filter and the corresponding dc output voltages and the ripple factors are measured and verified with the theoretical values.

EX. NO:

STUDY OF LOGIC GATES

AIM:

To verify the truth table of the logic gates AND, OR, NOT, EX-OR, NAND & NOR using ICs.

COMPONENTS REQUIRED:

IC 7432(OR Gate)

IC 7408(AND Gate)

IC 7404(NOT Gate)

IC 7400(NAND Gate)

IC 7402(NOR Gate)

Digital IC trainer kit

THEORY:

Logic gates are digital circuits with one or more input signals and only one output signal. Gates are digital circuits because the input and output signals are either low or high voltages. Gates are often called logic circuits because they can be analyzed using Boolean algebra.

PROCEDURE:

1. Connections are given as per the logic diagrams and the pin-out diagrams of the individual ICs.
2. Supply and ground connections are given to the ICs.
3. Inputs are applied by using the switches that provide the logic High and Low levels.
4. The outputs are observed by using the LED's.

AND Gate:

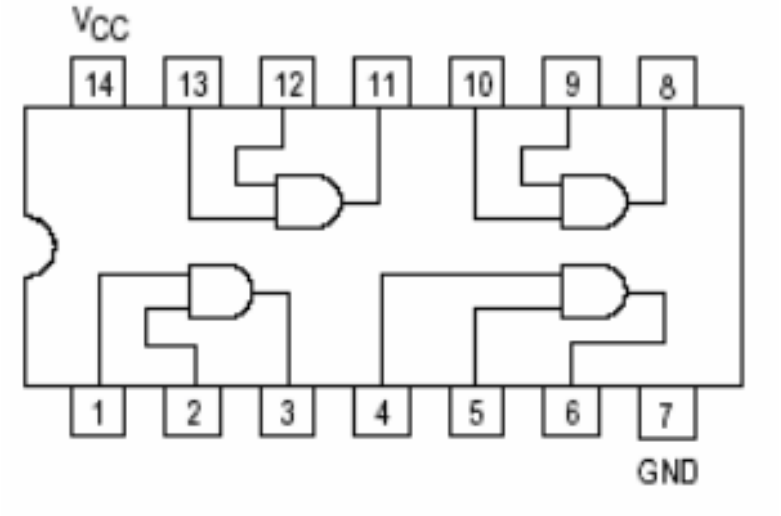
An AND gate can have two or more inputs but only one output. Its output can go to logic 1 if all its inputs are at the high state.

The Boolean expression for a two input AND gate is: F=x.y

TRUTH TABLE:

X	Y	OUTPUT F= XY
0	0	0
0	1	0
1	0	0
1	1	1

PIN DIAGRAM OF IC 7408 :



OR Gate:

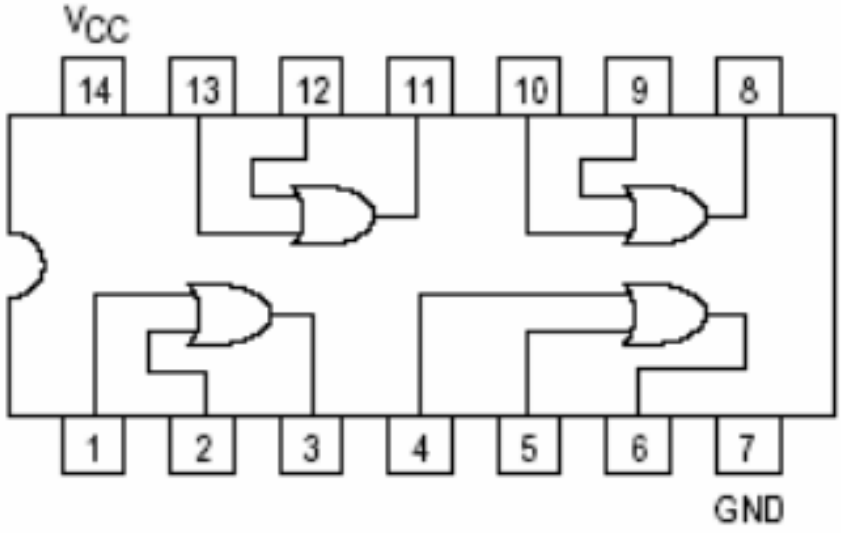
An OR gate can have two or more inputs but only one output. Its output will be at logic 1 if any or both of its inputs are at the high state.

The Boolean expression for a two input OR gate is: F = x + y

TRUTH TABLE:

X	Y	OUTPUT F= X+Y
0	0	0
0	1	1
1	0	1
1	1	1

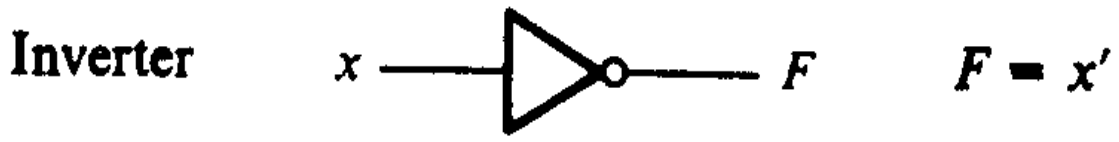
PIN DIAGRAM OF IC 7432 :



NOT Gate:

A NOT gate has a single input and a single output. It is also called as an inverter. The output will be at logic 1 if its input is at low state, otherwise its output will be at logic 0. Thus its output is the complement of its input.

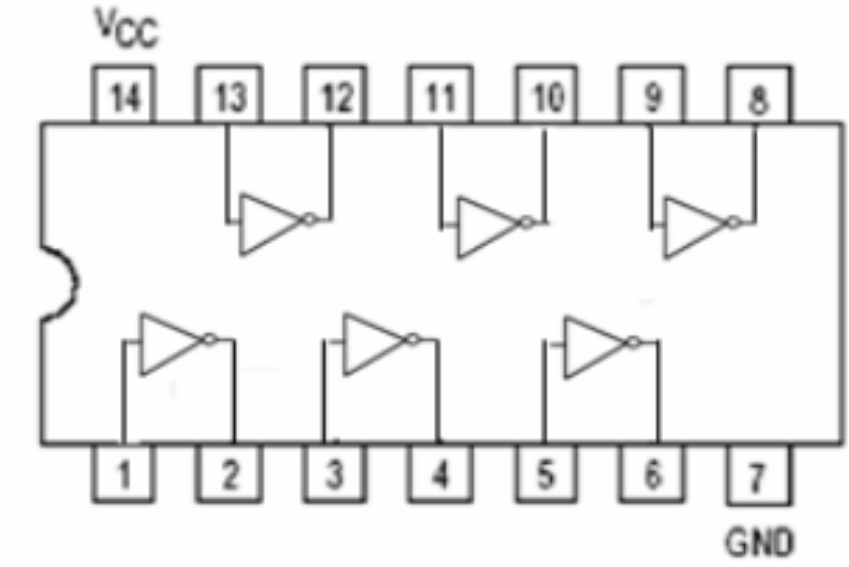
The Boolean expression for the inverter is: F = x'



TRUTH TABLE:

X	OUTPUT F= X'
0	1
1	0

PIN DIAGRAM OF IC 7404 :



NAND Gate:

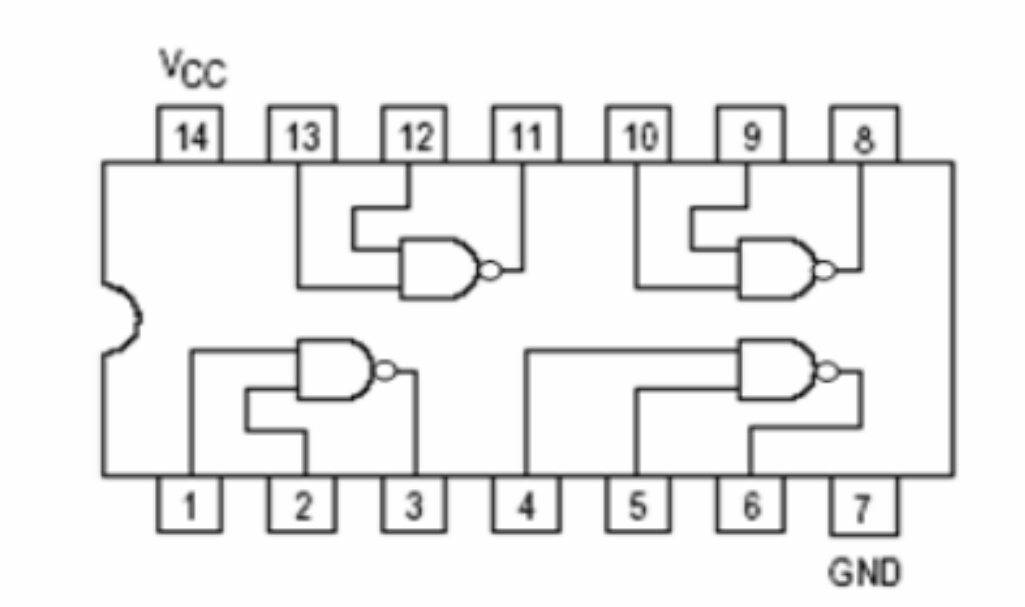
It is the combination of AND gate and NOT gate. It is also called as an universal gate. The output of this gate will go to logic 0 iff all its inputs are at the high state.

The Boolean expression for a two input NAND gate is F = (x.y)′

TRUTH TABLE:

X	Y	OUTPUT F= (XY)'
0	0	1
0	1	1
1	0	1
1	1	0

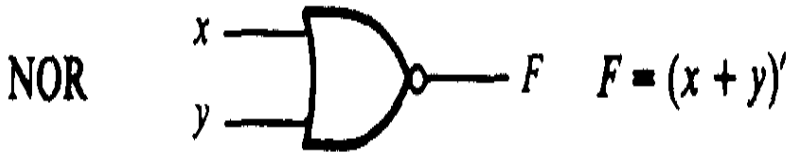
PIN DIAGRAM OF IC 7400 :



NOR Gate:

It is the combination of an OR gate and a NOT gate. It is also called as an universal gate. The output of this gate will go to logic 1 iff all its inputs are at the low state.

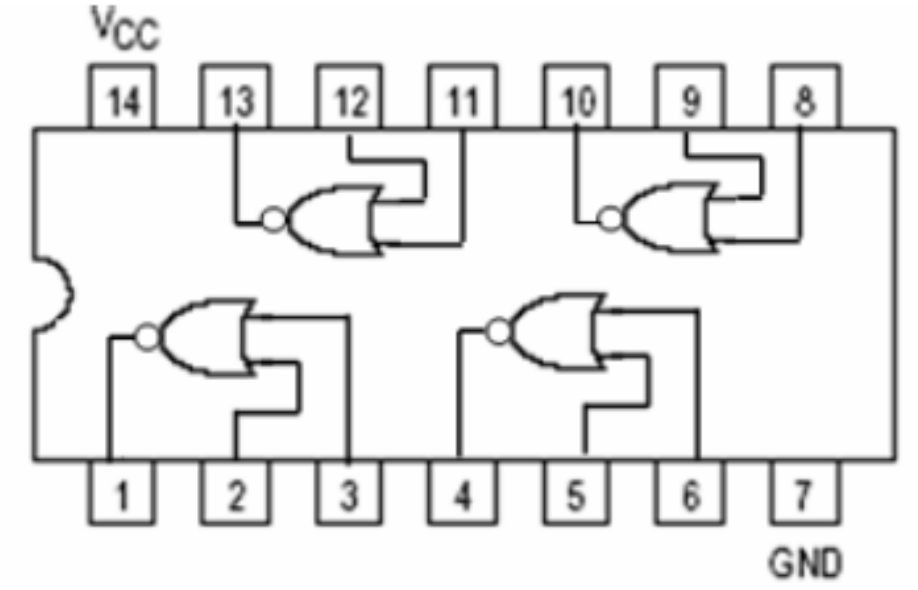
The Boolean expression for a two input NOR gate is: F = (x +y)′



TRUTH TABLE:

X	Y	OUTPUT F= (X+Y)'
0	0	1
0	1	0
1	0	0
1	1	0

PIN DIAGRAM OF IC 7402 :



EX-OR Gate:

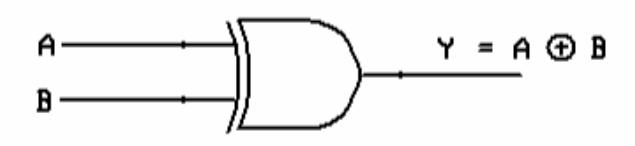
An EX-OR Gate performs the Boolean function,

$$A \oplus B = (A \cdot B') + (A' \cdot B)$$

It is similar to OR gate but excludes the combination of both A and B being equal to one. The EX-OR is a function that give an output signal '0' when the two input signals are equal either '0' or '1'.

EX-OR GATE

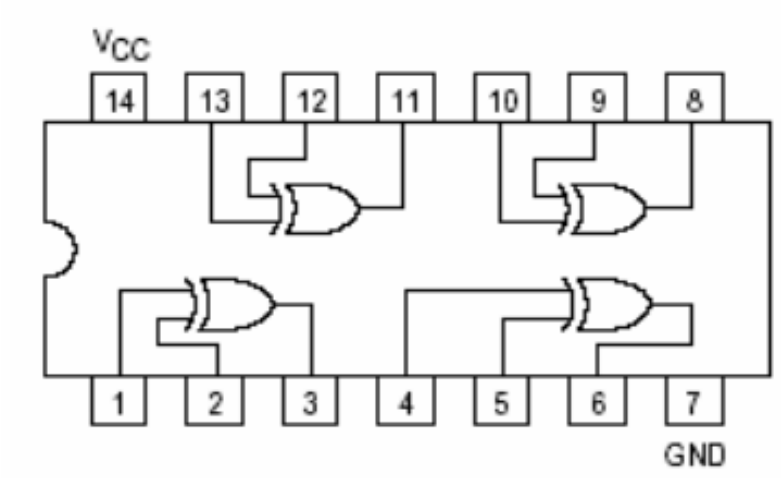
LOGIC DIAGRAM



TRUTH TABLE:

X	Y	OUTPUT Y = A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

PIN DIAGRAM OF IC 7486 :



RESULT:

Thus the logic gates are studied and it's truth tables are verified

Ex.No.

IMPLEMENTATION OF BINARY ADDER AND SUBTRACTOR

AIM:

To design and construct half adder, full adder, half subtractor and full subtractor circuits and verify the truth table using logic gates.

APPARATUS REQUIRED:

SL.NO.	COMPONENT	SPECIFICATION	QTY.
1.	AND GATE	IC 7408	1
2.	X-OR GATE	IC 7486	1
3.	NOT GATE	IC 7404	1
4.	OR GATE	IC 7432	1
5.	IC TRAINER KIT	-	1
6.	PATCH CORDS	-	23

THEORY:

HALF ADDER:

A half adder has two inputs for the two bits to be added and two outputs one from the sum ‘ S’ and other from the carry ‘ c’ into the higher adder position. Above circuit is called as a carry signal from the addition of the less significant bits sum from the X-OR Gate the carry out from the AND gate.

FULL ADDER:

A full adder is a combinational circuit that forms the arithmetic sum of input; it consists of three inputs and two outputs. A full adder is useful to add three bits at a time but a half adder cannot do so. In full adder sum output will be taken from X-OR Gate, carry output will be taken from OR Gate.

HALF SUBTRACTOR:

The half subtractor is constructed using X-OR and AND Gate. The half subtractor has two input and two outputs. The outputs are difference and borrow. The difference can be applied using X-OR Gate, borrow output can be implemented using an AND Gate and an inverter.

FULL SUBTRACTOR:

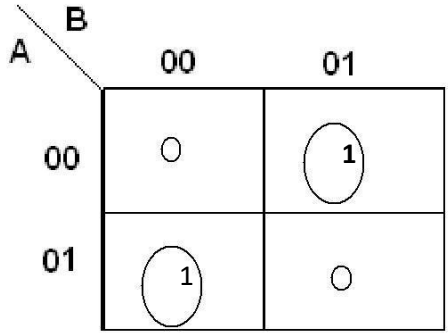
The full subtractor is a combination of X-OR, AND, OR, NOT Gates. In a full subtractor the logic circuit should have three inputs and two outputs. The two half subtractor put together gives a full subtractor .The first half subtractor will be C and A B. The output will be difference output of full subtractor. The expression AB assembles the borrow output of the half subtractor and the second term is the inverted difference output of first X-OR.

HALF ADDER

TRUTH TABLE:

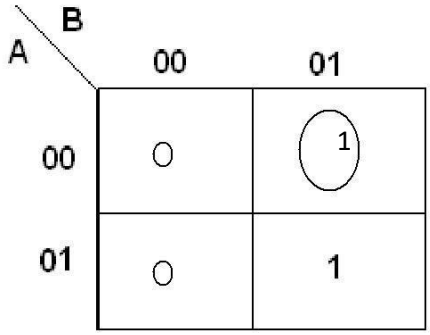
A	B	CARRY	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

K-Map for SUM:



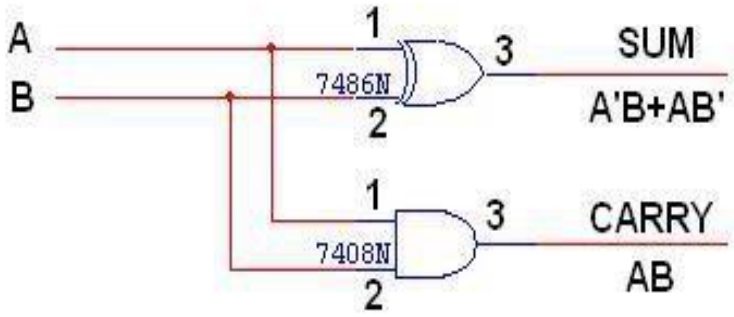
SUM = A'B + AB'

K-Map for CARRY:



CARRY = AB

LOGIC DIAGRAM:

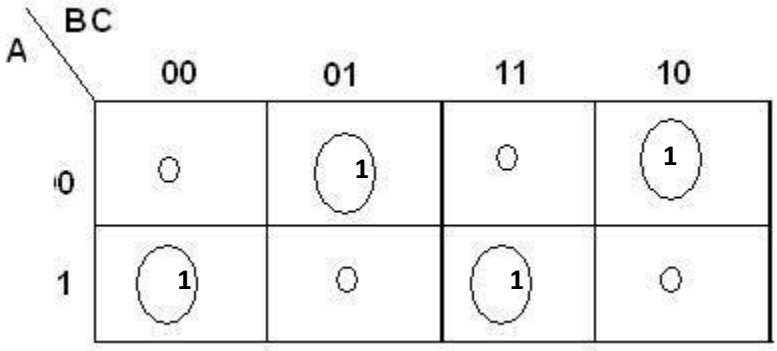


FULL ADDER

TRUTH TABLE:

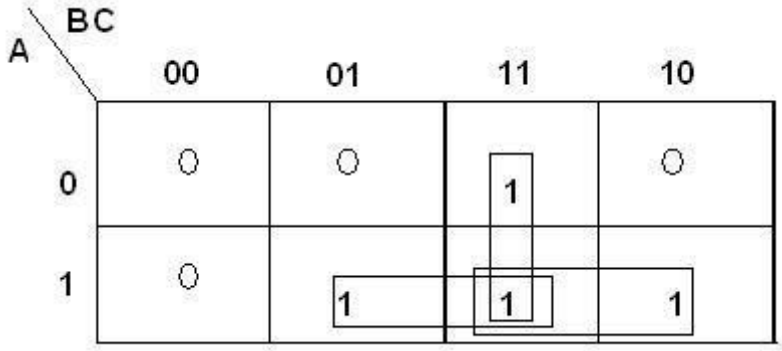
A	B	C	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

K-Map for SUM



SUM = A'B'C + A'BC' + ABC' + ABC

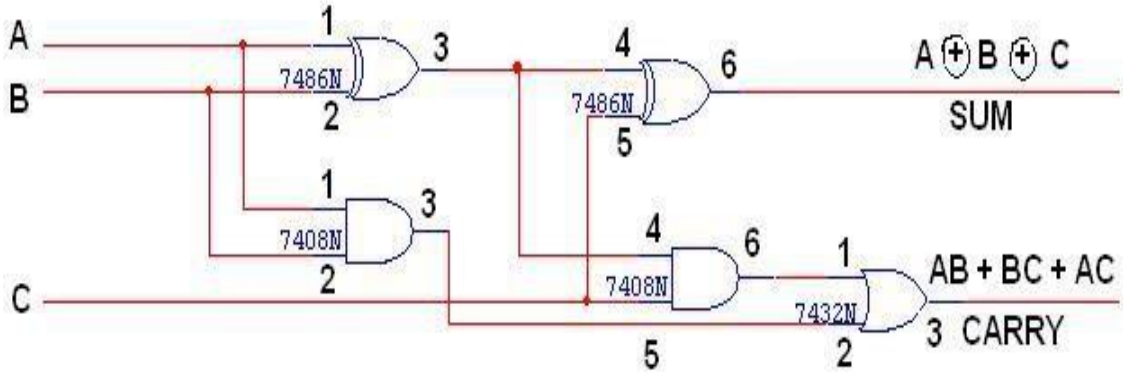
K-Map for CARRY



CARRY = AB + BC + AC

LOGIC DIAGRAM:

FULL ADDER USING TWO HALF ADDER

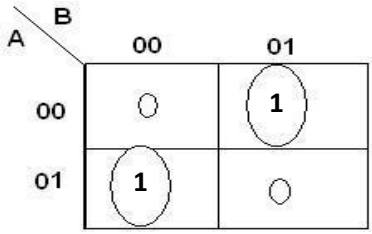


HALF SUBTRACTOR

TRUTH TABLE:

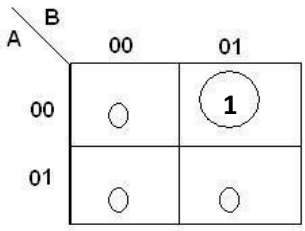
A	B	BORROW	DIFFERENCE
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

K-Map for DIFFERENCE



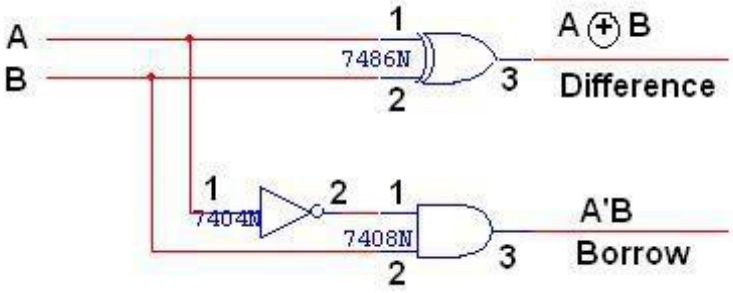
DIFFERENCE = A'B + AB'

K-Map for BORROW



BORROW = A'B

LOGIC DIAGRAM

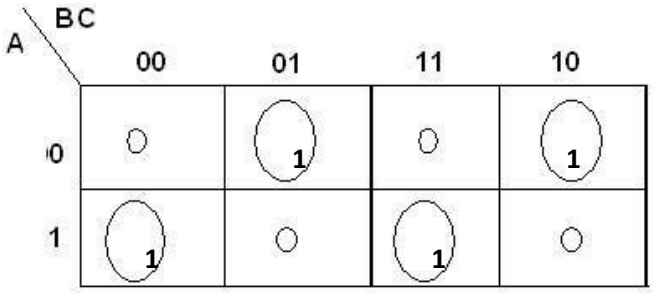


FULL SUBTRACTOR

TRUTH TABLE:

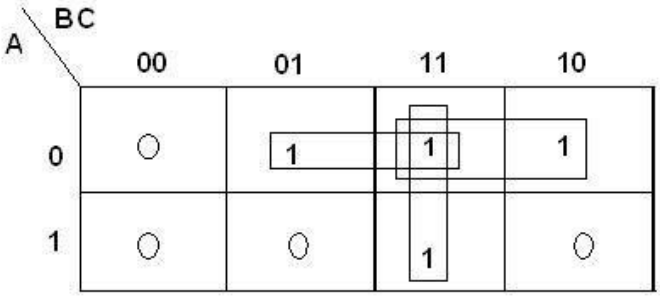
A	B	C	BORROW	DIFFERENCE
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

K-Map for Difference



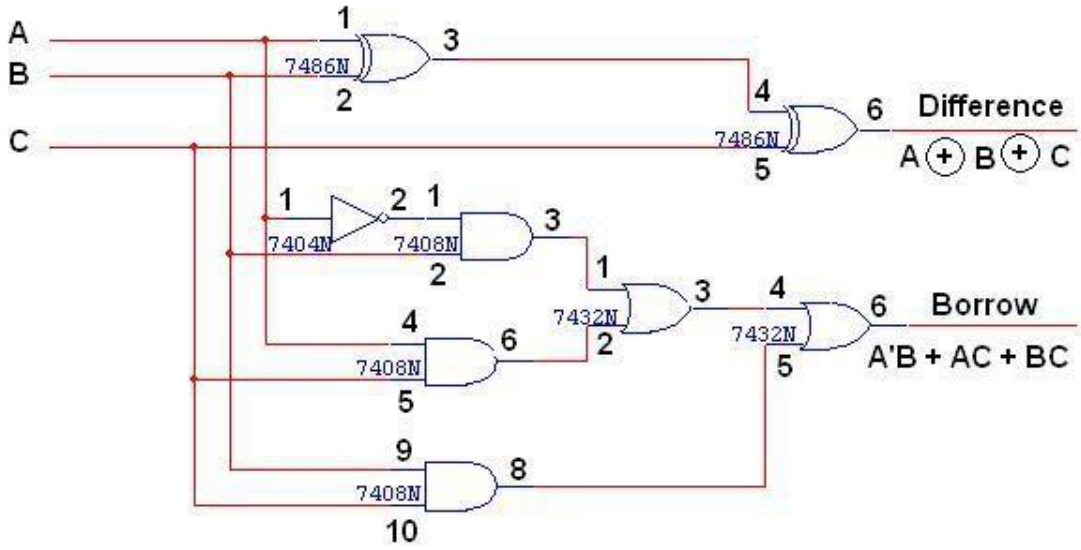
Difference = A'B'C + A'BC' + AB'C' + ABC

K-Map for Borrow

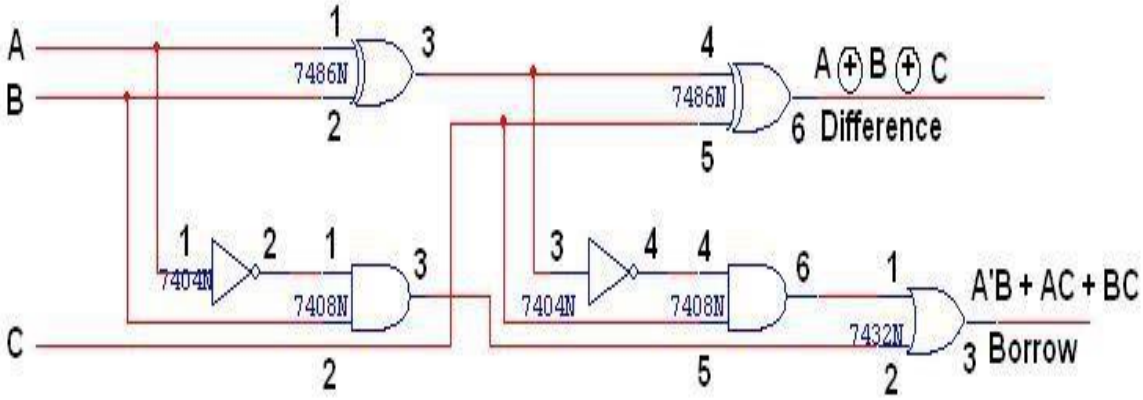


Borrow = A'B + BC + A'C

LOGIC DIAGRAM:



FULL SUBTRACTOR USING TWO HALF SUBTRACTOR



PROCEEDURE:

(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.

(iii) Observe the output and verify the truth table.

RESULT:

Thus, the half adder, full adder, half subtractor and full subtractor circuits are designed, constructed and verified the truth table using logic gates.

Ex. No. **STUDY OF DIGITAL STORAGE OSCILLOSCOPE**

AIM:

To Study the working and functions of digital storage oscilloscope.

THEORY:

An oscilloscope (also known as a scope, CRO, DSO or, an O-scope) is a type of electronic test instrument that allows observation of constantly varying signal voltages, usually as a two-dimensional graph of one or more electrical potential differences using the vertical or 'Y' axis, plotted as a function of time, (horizontal or 'x' axis). Although an oscilloscope displays voltage on its vertical axis, any other quantity that can be converted to a voltage can be displayed as well. In most instances, oscilloscopes show events that repeat with either no change, or change slowly. Oscilloscopes are commonly used to observe the exact wave shape of an electrical signal. In addition to the amplitude of the signal, an oscilloscope can show distortion, the time between two events (such as pulse width, period, or rise time) and relative timing of two related signals.[1] Oscilloscopes are used in the sciences, medicine, engineering, and telecommunications industry. General-purpose instruments are used for maintenance of electronic equipment and laboratory work. Special-purpose oscilloscopes may be used for such purposes as analyzing an automotive ignition system, or to display the waveform of the heartbeat as an electrocardiogram. Originally all oscilloscopes used cathode ray tubes as their display element and linear amplifiers for signal processing, (commonly referred to as CROs) however, modern oscilloscopes have LCD or LED screens, fast analog-to-digital converters and digital signal processors. Although not as commonplace, some oscilloscopes used storage CRTs to display single events for a limited time. Oscilloscope peripheral modules for general purpose laptop or desktop personal computers use the computer's display, allowing them to be used as test instruments.

Display and general external appearance The basic oscilloscope, as shown in the illustration, is typically divided into four sections: the display, vertical controls, horizontal controls and trigger controls. The display is usually a CRT or LCD panel which is laid out with both horizontal and vertical reference lines referred to as the graticule. In addition to the screen, most display sections are equipped with three basic controls, a focus knob, an intensity knob and a beam

finder button. The vertical section controls the amplitude of the displayed signal. This section carries a Volts-per-Division (Volts/Div) selector knob, an AC/DC/Ground selector switch and the vertical (primary) input for the instrument. Additionally, this section is typically equipped with the vertical beam position knob. The horizontal section controls the time base or “sweep” of the instrument. The primary control is the Seconds-per-Division (Sec/Div) selector switch. Also included is a horizontal input for plotting dual X-Y axis signals. The horizontal beam position knob is generally located in this section. The trigger section controls the start event of the sweep. The trigger can be set to automatically restart after each sweep or it can be configured to respond to an internal or external event. The principal controls of this section will be the source and coupling selector switches. An external trigger input (EXT Input) and level adjustment will also be included. In addition to the basic instrument, most oscilloscopes are supplied with a probe as shown. The probe will connect to any input on the instrument and typically has a resistor of ten times the oscilloscope's input impedance. This results in a .1 (-10X) attenuation factor, but helps to isolate the capacitive load presented by the probe cable from the signal being measured. Some probes have a switch allowing the operator to bypass the resistor when appropriate.

PROCEDURE:

Measurement of Voltage

A voltage can be measured by noting the Y deflection produced by the voltage; using this deflection in conjunction with the Y-gain setting, the voltage can be calculated as follows:

V = (no. of boxes in cm.) x (selected Volts/cm scale)

Measurement of Frequency

A simple method of determining the frequency of a signal is to estimate its periodic time from the trace on the screen of a CRT. However, this method has limited accuracy, and should only be used where other methods are not available. To calculate the frequency of the observed signal, one has to measure the period, i.e. the time taken for 1 complete cycle, using the calibrated sweep scale. The period could be calculated by

T = (no. of squares in cm) x (selected Time/cm scale)

Once the period T is known, the frequency is given by f (Hz) = 1/T(sec)

S. No.	TYPE OF WAVE	TIME (SEC)	AMPLITUDE (V)	SET FREQUENCY(Hz)	MEASURED FREQUENCY $= \frac{1}{TIME}$ Hz
1	SINE				
2	RAMP				
3	SQUARE				

RESULT:

Thus the function of digital storage oscilloscope such as measurement of voltage and frequency was studied.